# User's Guide

Publication number E8033-97001, September 2001



For Safety information, Warranties, and Regulatory information, see the pages behind the index.

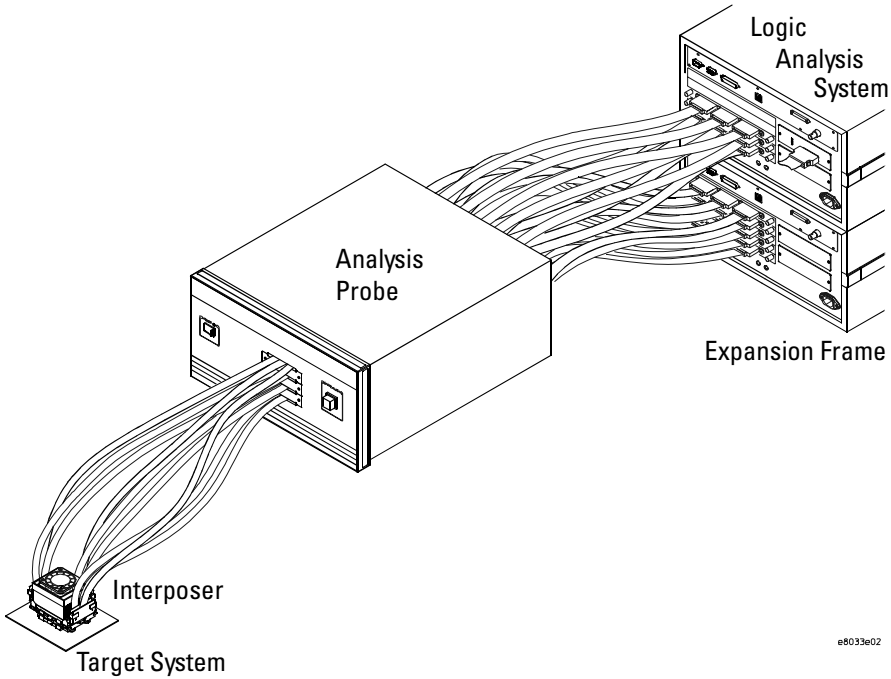
# 423-Pin IA-32 Analysis Probe

# Agilent Analysis Probe for the 423-Pin IA-32 Processor—At a Glance

The Agilent E8033A analysis probe provides a complete interface for state analysis between Intel® IA-32 processors and Agilent logic analyzers. This manual describes how to connect an Agilent logic analysis system to your target system. The product consists of several components: an analysis probe (with its attached cables and interposer) and software for the logic analysis system.

## Analysis Probe

The analysis probe and interposer provide the physical connection between the target microprocessor and the logic analyzer. The configuration software sets up the logic analyzer for compatibility with the analysis probe. The analysis probe must be used with Agilent 16715/16/17/18/19A or 16750/51/52A logic analyzer modules in an Agilent 16700-series logic analysis system and expansion frame.



# In This Book

This book documents the following products:

| Product ordered | Includes |
|---|---|
| E8033A | Analysis probe, interposer, software, and accessories for the Intel® 423-pin IA-32 processor. |

# Additional Information Sources

Additional or updated information can be found in the following places:

Newer editions of this manual may be available. Contact your local Agilent representative.

The **measurement examples** include valuable tips for making analysis measurements. You can find the measurement examples under the system help in your 16700-series logic analysis system.

# Contents

# Part 1

# Installation Guide

# Overview of Installation and Setup

Follow these general steps to connect your equipment.

> Be sure to read all of the installation instructions, with special attention to the precautions required to prevent equipment damage. Note that this manual also contains instructions for disconnecting the equipment.

1. Check that you received all of the necessary equipment. See “Equipment and Requirements” on page 13..
2. Prepare the target system and the space around the target system. See “Preparing the Target System” on page 17.
3. Install logic analyzer modules in your logic analysis system, if necessary. See “Installing Logic Analyzer Modules” on page 23.
4. Make the physical connections to probe the target system. This includes installing the interposer between the microprocessor and the socket on the target system, and connecting the cables from the logic analyzer to the analysis probe. See the "Probing the Target System" chapter.
5. Turn on the logic analysis system.
6. Install the software. See “Installing Software” on page 24.
7. Turn on the analysis probe, then the target system. See “Power-ON/ Power-OFF Sequence” on page 22.
8. Load a configuration file. See “Loading Configuration Files” on page 51.
9. Begin making measurements.

# 1

# Equipment and Requirements

This chapter lists the equipment which is included with your analysis probe, and the additional equipment you need to make measurements.

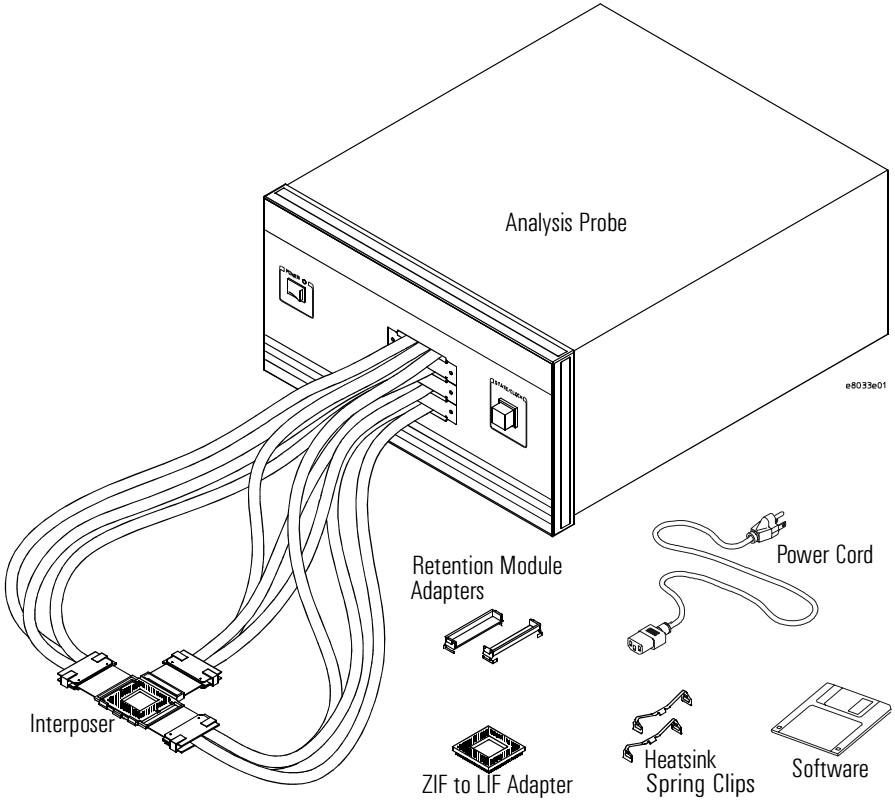
# Equipment Supplied

This section lists equipment supplied with the analysis probe and equipment requirements for using the analysis probe.

The equipment supplied with the analysis probe is listed below:

- E8033B analysis probe
- Analysis probe cables, attached to the analysis probe.
- Interposer, attached to the analysis probe cables.
- Pin protector. The interposer is shipped plugged into a ZIF socket to protect the pins from damage. Leave this pin protector in place until you plug the interposer into the target system.
- ZIF-to-LIF adapter
- Retention module adapters to support the heatsink when the interposer is in place.
- Heatsink spring clips to hold the processor and interposer in place. These clips have been modified to work with the Agilent interposer.
- Logic analyzer configuration files, and merge tool software on floppy disk.
- This *User's Guide*.
- Power cord for the analysis probe.

  If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office. Use only the power cord supplied with the analysis probe.


Analysis Probe
e8033e01
Retention Module
Adapters
Power Cord
Interposer
ZIF to LIF Adapter
Heatsink
Spring Clips
Software

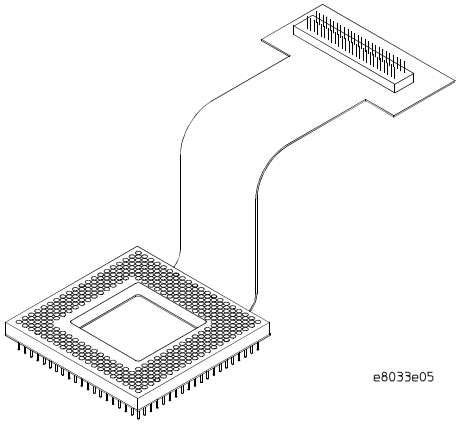
## Additional equipment and software required

In addition to the items supplied with the analysis probe, you need all of the following items:

- An Agilent 16700-series logic analysis system with operating system revision 2.40 or greater.
- An  Agilent expander frame.
- At least eight Agilent 16715/16/17/18/19A or 16750/51/52A logic analyzer modules.

## Optional equipment supported

- Agilent E8033A Option 001 ITP interposer.



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# Preparing the Target System

This chapter describes the factors you need to consider when designing and preparing the target system for logic analysis with the 423-Pin IA-32 Analysis Probe.

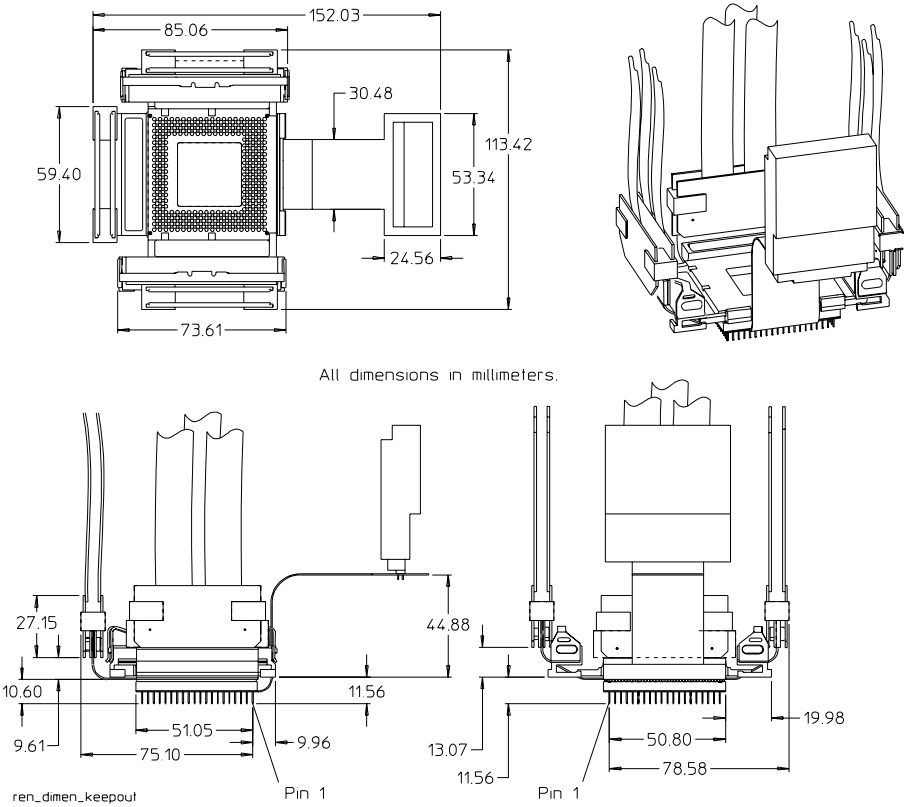
# Mechanical Requirements

## Keep-Out Area On the Target Board

The interposer extends slightly beyond the area normally occupied by the microprocessor. It is important to keep components from interfering with the interposer in this restricted area.

## Analysis Probe Dimensions

The following illustration shows the approximate dimensions of the interposer. Design changes may result in slight variations from these dimensions.



## Clearance above the Target Board

Be careful to allow adequate space above the target board for the analysis probe, and for egress of the analysis probe cables.

The height of the paddles on the end of the analysis probe cables above the socket on the target system is 3 inches.

## Heatsink Requirements

The interposer is shipped with retention module adapters and modified heatsink spring clips which are designed to work specifically with the Intel-recommended heatsink.

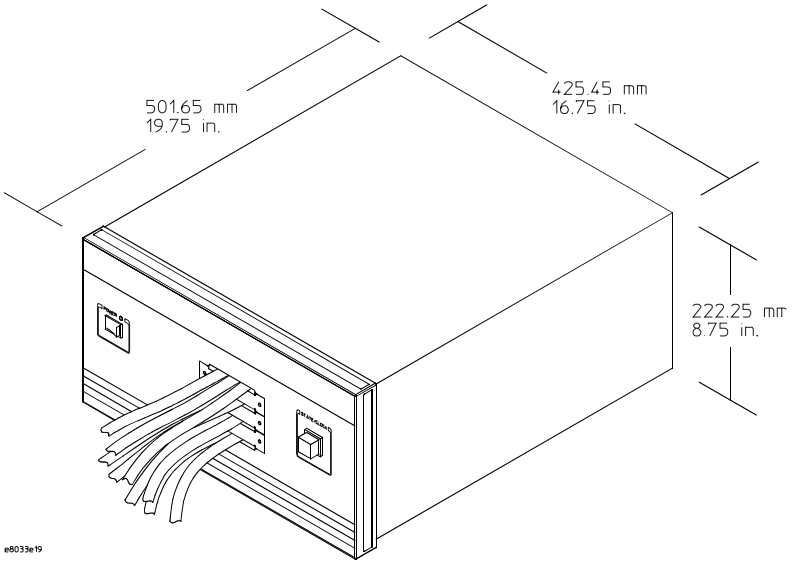
If you use a heatsink of your own design, pay close attention to the keep-out area requirements on the previous page.

# Bench Space for the Analysis Probe

Take care to allow space for the analysis probe be placed near the target system and the logic analysis system. You will also need plenty of space behind the analysis probe for the logic analysis system and expander frame.

Allow at least 5 cm clearance on both sides of the analysis probe for proper cooling.

**CAUTION:** Do not block the airflow holes on the sides of the analysis probe box. Blocked airflow may cause overheating and equipment damage



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# Setting Up the Logic Analysis System

This chapter shows you how to power on the logic analysis system, how to set up the logic analyzer modules, and how to install the software.

# Power-ON/Power-OFF Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

Use only the power cord supplied with the analysis probe.

## To power-ON

Ensure the target system is powered off.

1. Turn on the logic analysis system.
2. Turn on the analysis probe.
3. When the logic analyzer is connected to the target system, and everything is configured, turn on your target system.

## To power-OFF

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off the analysis probe.
3. Turn off your logic analysis system.

## To cycle power on the target system

- Cycle power on the target system only. You do not need to turn off the analysis probe or logic analysis system.

# Installing Logic Analyzer Modules

You should install logic analyzer, oscilloscope, or pattern generator modules in your logic analysis system before you begin make connections or configure the logic analysis system.

Three logic analyzer cards in the main logic analysis system frame must be connected together as one machine. These cards must be placed in the lower three slots in the frame.

Five cards in the expander frame must be connected together as one machine.

All of the cards in a machine should be of the same type.

Here are examples of valid and invalid configurations:

| Main Frame | Expander Frame | |
|---|---|---|
| Oscilloscope | 16717A | Yes |
| 16715A | 16717A | |
| 16719A | 16717A | |
| 16719A | 16717A | |
| 16719A | 16717A | |

| Main Frame | Expander Frame | |
|---|---|---|
| | 16719A | No |
| 16719A | 16717A | |
| 16719A | 16717A | |
| 16719A | 16717A | |
| | 16717A | |

**See Also**

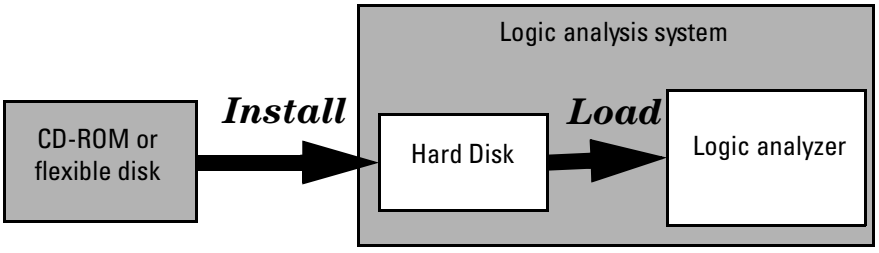
Refer to the Agilent 16700-series logic analysis system's *Installation Guide*.

# Installing Software

This chapter explains how to install the software you will need for your analysis probe.

## Installing and loading

Installing the software will copy the files to the hard disk of your logic analysis system. Later, you will need to load some of the files into the logic analyzer module.




## What needs to be installed

Install the software from the following floppy disks:

1. Logic analysis system operating system patches, if applicable.
2. Merge tool.
3. Logic analysis system configuration files.

> Install the disks in the order listed above.

The logic analysis system will end the current session after installing the patch and again after installing the merge tool.

## To install software from floppy disk

Installing a processor support package will take just a few minutes.

1. Insert the first disk in the drive.
2. Select the System Admin icon.
3. Select the Software Install tab.
4. Select Install... .

   Change the media type to “Floppy Disk” if necessary.
5. Select Apply.
6. Select the software package.

   Since you are installing from a floppy disk,only one package will be listed.
7. Select Install.

   The Continue dialog box will appear.
8. Select Continue.

   The dialog box will display “Progress: completed successfully” when the installation is complete.
9. If required, the system will automatically reboot. Otherwise, close the software installation windows.

   The configuration files are stored in /logic/configs/hp/*processor*.

   The inverse assemblers are stored in /logic/ia.

**See Also**

The on-line help for more information on installing, licensing, and removing software.

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# Probing the Target System

This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

This chapter explains how to connect the Agilent E8033A analysis probe to the target system.

## Overview

Connecting the analysis probe to the target system consists of the following steps:

- Step 1: Remove the heatsink from the microprocessor (page 30).
- Step 2: Remove the microprocessor from the target system (page 31).
- Step 3: Install the ZIF-to-LIF adapter on the target system (page 32).
- Step 4: Install the interposer on the target system (page 34).
- Step 5: Attach the processor to the interposer (page 36).
- Step 6: Re-install the heatsink (page 38).
- Step 7: Connect the analysis probe to the logic analyzer (page 40).

**CAUTION:** To prevent equipment damage, remove power from the target system and analysis probe before making attachments.

**Protecting the Interposer**

Here is a summary of precautions to take to avoid damaging the interposer:

DO leave the analysis probe cables connected to the interposer.

DO minimize the removal of the interposer, once it is connected to the microprocessor and target system.

DO exercise patience and care when working with the interposer.

DO use the supplied removal tool to pull the interposer from the ZIF-to-LIF adapter.

DO use ESD precautions.

DO NOT insert any kind of tool between the interposer and the microprocessor, except as described in this manual.

DO NOT pull on or twist the "wings" of the interposer.

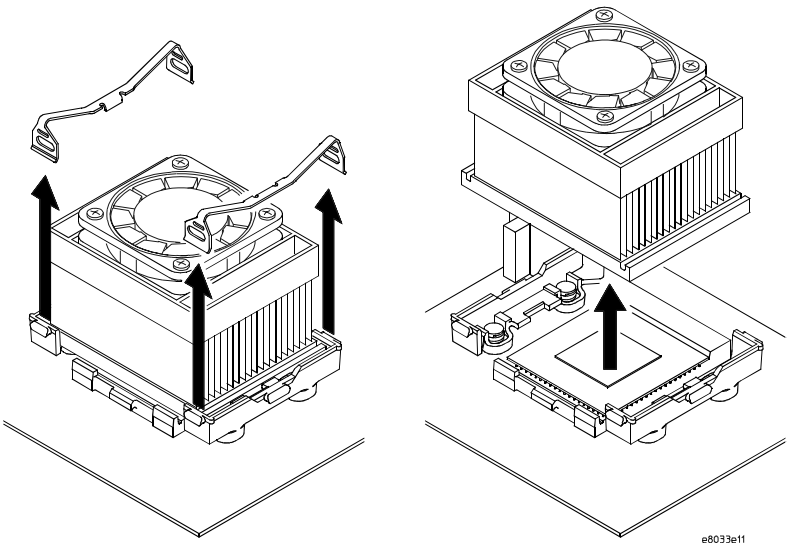
## Step 1: Remove the heatsink from the microprocessor

1 Unplug the power cable from the heatsink.

2 Remove the heatsink spring clips.

Keep the spring clips in a safe place. You will need them to reinstall the microprocessor without the analysis probe. You may want to label the clips, so they won't get mixed up with the clips which come with the analysis probe.

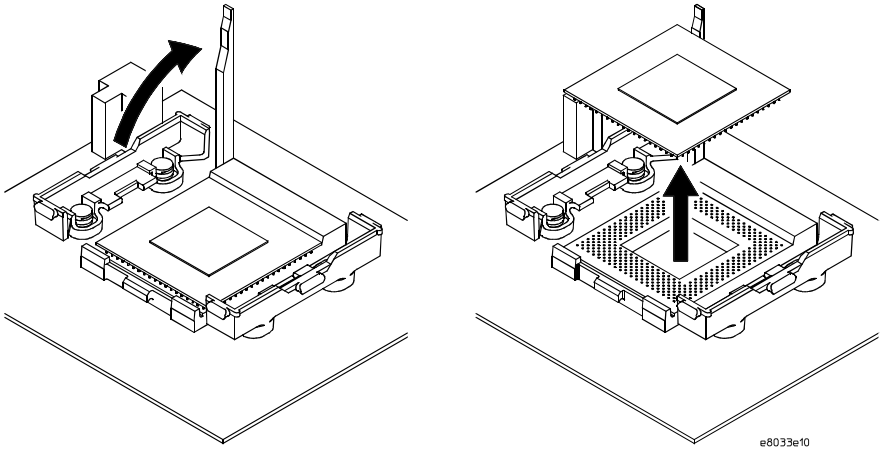
3 Gently twist the heatsink to break the bond of the thermal paste, then lift the heatsink from the processor.



## Step 2: Remove the microprocessor from the target system

**CAUTION:** Turn off all power to the target system. To prevent equipment damage, physically disconnect all power sources from the target system before removing or installing any components.

1. Lift the arm on the target system's ZIF socket.
2. Lift the microprocessor straight up.



## Step 3: Install the ZIF-to-LIF adapter on the target system

- If you are using the option 001 ITP interposer, install it now.

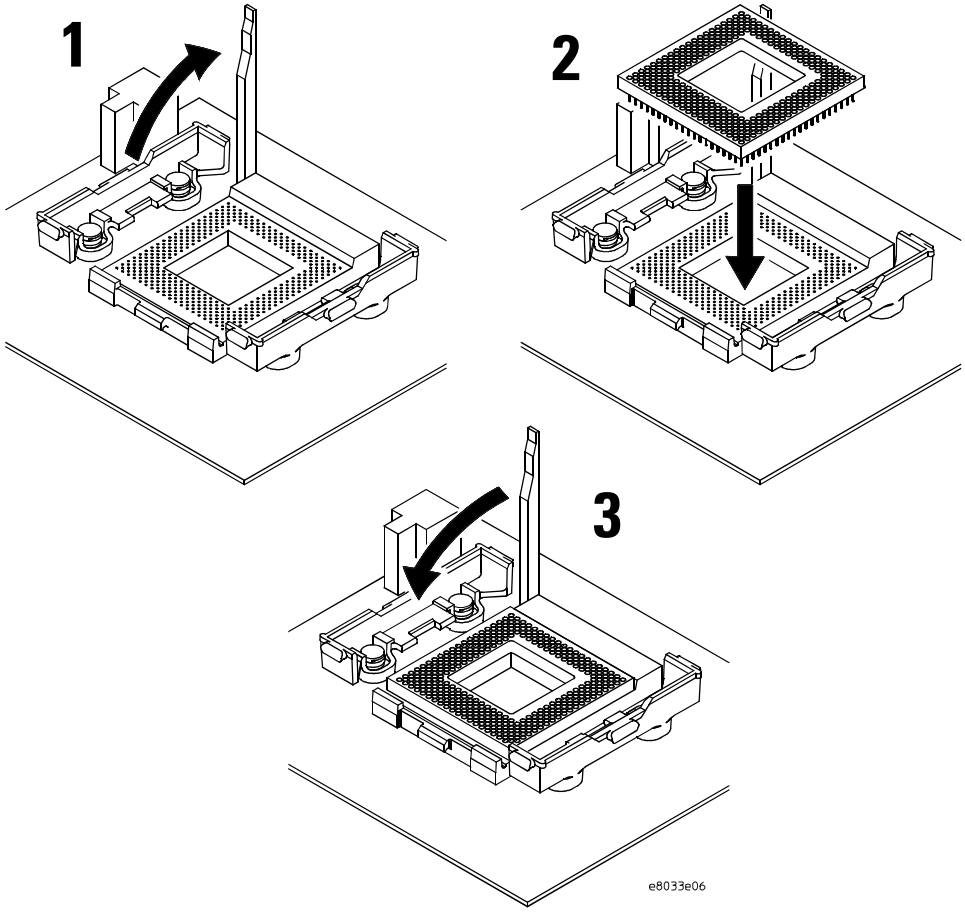
  Follow the instructions in the Installation Guide which came with the interposer. If you are using the ITP interposer, you do not need to install the ZIF-to-LIF adapter.

- If you are not using the option 001 ITP interposer, install the ZIF-to-LIF adapter:

1. Lift the arm of the ZIF socket on the target system.
2. Insert the ZIF-to-LIF adapter.

   The adapter can only be inserted one way—the number of rows of pins is different along one side of the socket.
3. Close the arm of the ZIF socket.

The ZIF-to-LIF adapter or ITP interposer is required to provide clearance above the target system for the interposer.


1
2
3
e8033e06

## Step 4: Install the interposer on the target system

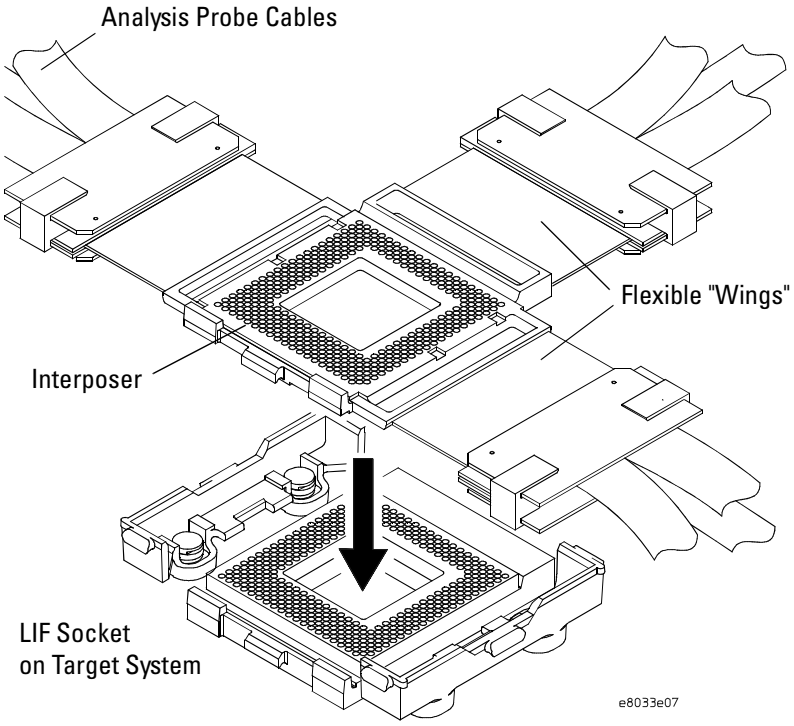
**CAUTION:** Ensure that the interposer pins are perfectly aligned with the socket before you press the microprocessor cartridge/interposer assembly into the socket. If not aligned correctly, the pins on the interposer will break. Unlike the microprocessor, the interposer does not have tabs which mate with notches on the socket to ensure correct alignment.

**CAUTION:** Do not kink the analysis probe cables. Kinking the analysis probe cables will change the calibration, and the analysis probe will have to be returned for repair and recalibration.

1. Bend the flexible "wings" of the interposer upward so that the analysis probe cables fit between the components on your target system.
2. Align the interposer over the socket on the target system.
3. Gently wiggle the assembly until you feel the pins fall into the holes.
4. Visually check that the pins are aligned over the correct holes.

   Take your time, and check very carefully.
5. Press straight down, applying pressure evenly over the socket.

   Apply no more than 15 lbs of pressure. You will feel a sudden "give" when the interposer seats into the ZIF-to-LIF adapter.




Note: The analysis probe cables should remain attached to the interposer throughout the installation process.

## Step 5: Attach the processor to the interposer

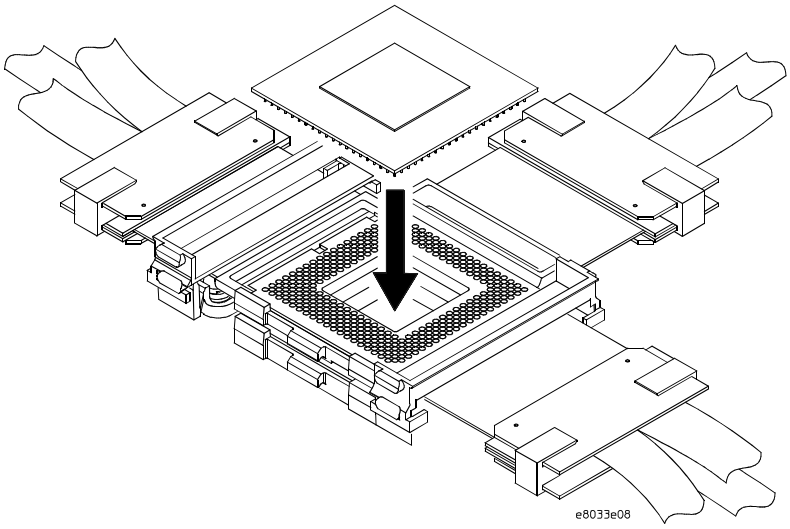
**CAUTION:** Use ESD precautions. Electrostatic discharge (ESD) can damage the interposer, as well as the target system. Use grounded wrist straps and mats when you handle the interposer.

**CAUTION:** Be very careful when handling the interposer. Do not bend the pins on the interposer.

1. Align the processor over the socket on the interposer.
2. Gently wiggle the assembly until you feel the pins fall into the holes.
3. Visually check that the pins are aligned over the correct holes.

   Take your time, and check very carefully.
4. Press straight down, applying pressure evenly over the processor.

   Apply no more than 15 lbs of pressure.

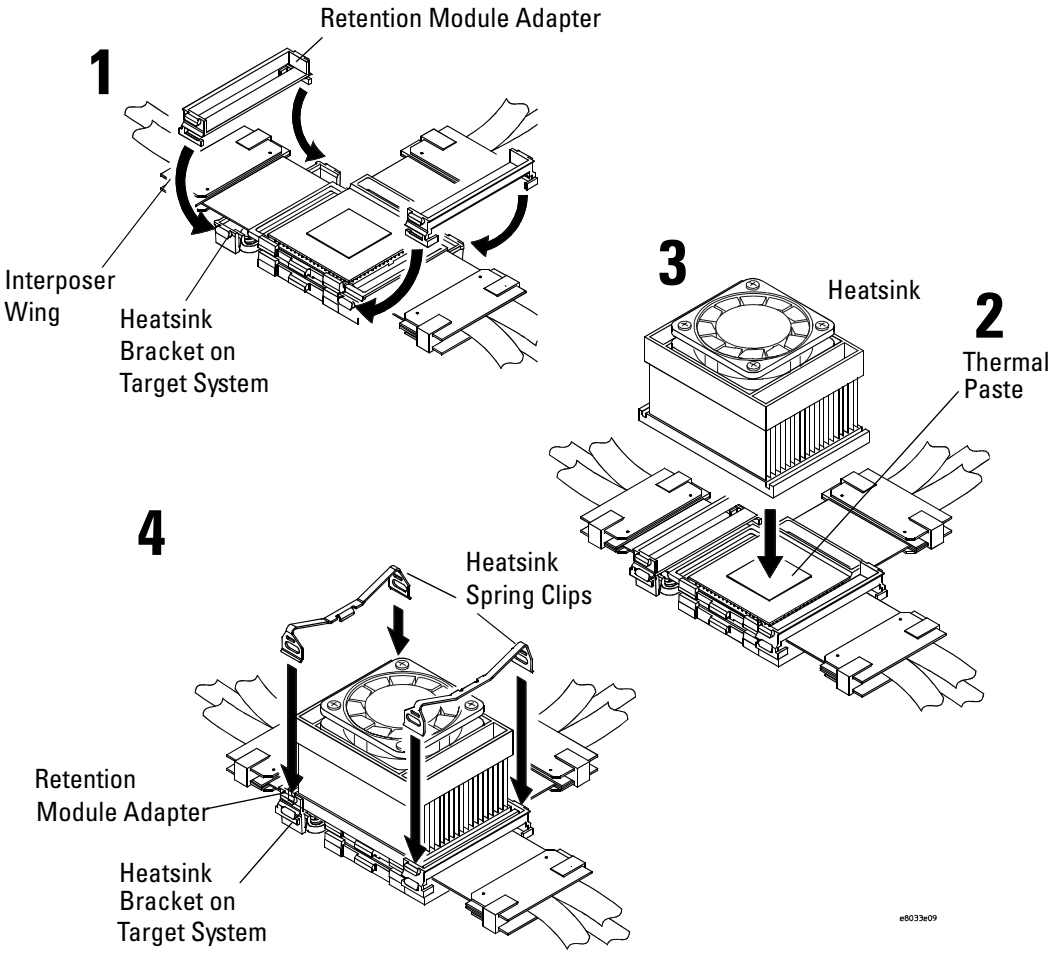

e8033e08

## Step 6: Re-install the heatsink

1. Slip the retention module adapters over "wings" of the interposer, and slide the adapters onto the ZIF socket.
2. Check that there is sufficient thermal paste on the top of the processor or on the bottom of the heatsink.
3. Place the heatsink on the processor.
4. Install the heatsink spring clips to hold the heatsink in place.

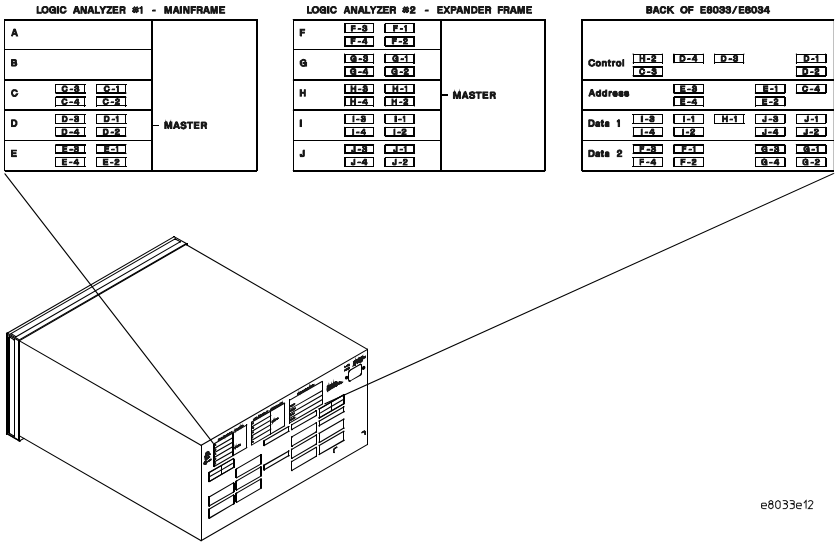
   Use the spring clips which were supplied with the analysis probe. They are taller than the normal spring clips.

   The spring clips attach to the retention module adapters.
5. Plug the power cord back into the heatsink.


Retention Module Adapter
1
Interposer
Wing
Heatsink
Bracket on
Target System
3
Heatsink
2
Thermal
Paste
4
Heatsink
Spring Clips
Retention
Module Adapter
Heatsink
Bracket on
Target System
e8033e09

## Step 7: Connect the analysis probe to the logic analyzer

- Connect the pod cables to the connectors on the analysis probe as shown on the back of the analysis probe.



# Uninstalling the analysis probe

**CAUTION:** To maximize the life of the interposer and LIF socket, minimize uninstalling and reinstalling the interposer.

**CAUTION:** Leave the analysis probe cables attached to the interposer.

**CAUTION:** Use ESD precautions. Electrostatic discharge (ESD) can damage the interposer, as well as the target system. Use grounded wrist straps and mats when you handle the interposer.

1. Remove power from the target system and from the analysis probe.

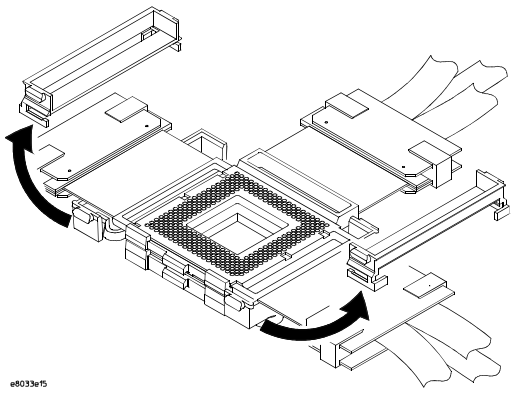
   You may leave the logic analysis system turned on.

2. Remove the heatsink and retention module adapters (page 42).
3. Remove the processor from the interposer (page 43).
4. Remove the interposer from the target system (page 44).
5. Remove the ZIF-to-LIF adapter from the target system (page 46).
6. Re-install the processor on the target system.

## To remove the heatsink from the processor on the interposer

1 Remove the spring clips.

2 Remove the retention module adapters.



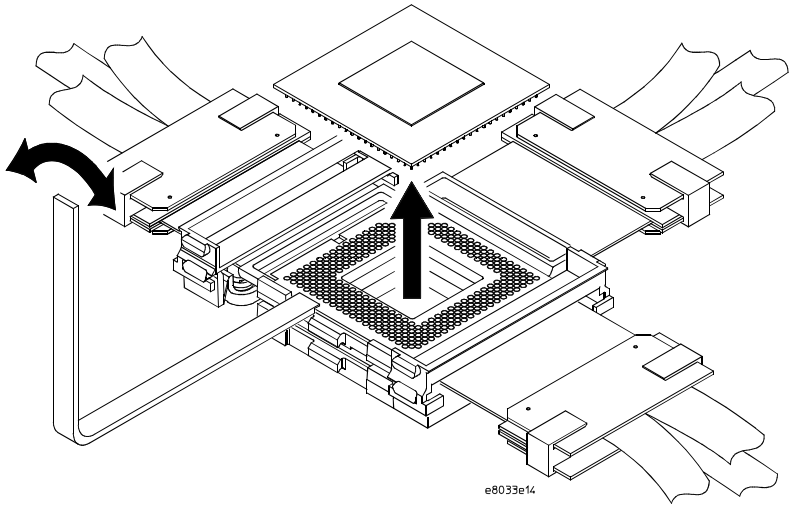

3 Lift the heatsink from the processor.

## To remove the processor from the LIF socket on the interposer

The pry tool provided with your analysis probe is used to remove the microprocessor from your interposer.

**CAUTION:** Use a twisting motion rather than a prying motion. Prying will be ineffective and can cause damage to the interposer.

1. Start at a corner of the socket and lift a small amount.
2. Move down the row of pins and lift some more.
3. Proceed around all four sides, until the processor is free.
4. Lift the processor from the socket.




Note: The analysis probe cables should remain attached to the interposer throughout the installation/uninstallation process.

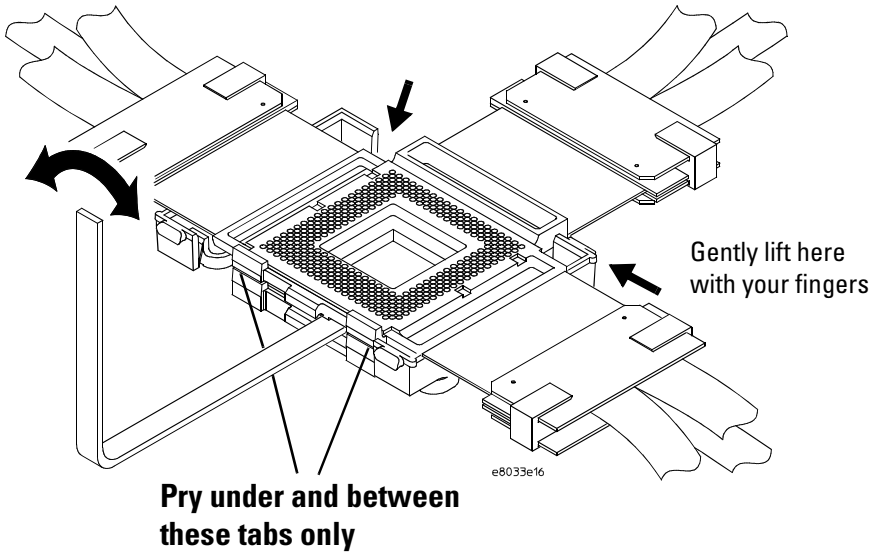
## To remove the interposer from the LIF socket on the target system

**CAUTION:** Pry only along the open edge of the interposer. Resistors are attached under the "wings" of the interposer. If you use any kind of tool under the wings, these resistors may be damaged.

**CAUTION:** Use ESD precautions. Electrostatic discharge (ESD) can damage the interposer, as well as the microprocessor. Use grounded wrist straps and mats when you handle the interposer.

**CAUTION:** Be very careful when handling the interposer. Do not bend the pins on the interposer.

**1** Along the open side of the interposer, pry one corner of the interposer a little bit..



**2** Pry the other corner of the interposer a little bit.

Pry just enough to loosen the interposer, but not enough to completely free the pins from the socket.

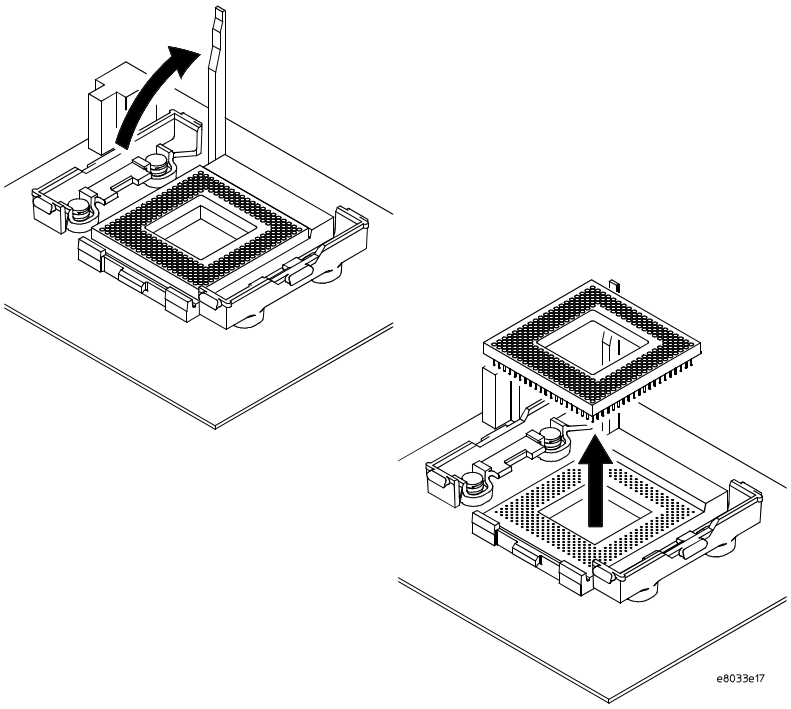
**3** Gently lift the wing of the interposer which is opposite the open side.

Note: The analysis probe cables should remain attached to the interposer throughout the installation/uninstallation process.

## To remove the ZIF-to-LIF adapter from the target system

Once the interposer has been removed from the ZIF-to-LIF adapter:

1. Lift the arm on the target system's ZIF socket.
2. Lift the adapter straight up.




You can now install the microprocessor in the ZIF socket on the target system.

# Part 2

# Using the Logic Analyzer

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# Configuring the Logic Analysis System

This chapter shows you how to load configuration files, which set up the logic analysis system for your microprocessor, and how to further configure the software before you begin making measurements.

# Configuring the Logic Analyzer

Analysis features are determined by a combination of analysis probe operating mode settings and options selected in the Agilent 16700 Listing window under the "Invasm - Filter..." and "Invasm - Preferences..." menus. The Filter dialog (page 80) allows the user to show, suppress, or change the color of an entire acquisition state.

# Loading Configuration Files

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer.

There is only one configuration file.

## To load configuration files

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /logic/configs/hp/E8033A exists.

> If the above directory does not exist, see "To install software from floppy disk" on page 25.

2 Using File Manager, select the configuration file from the /logic/configs/hp/E8033A directory, then click Load.

The logic analyzer is configured for IA-32 analysis by loading the appropriate configuration file. Loading configuration files also automatically sets up the workspace.

3 Close File Manager.

## To create your own configuration files

If you create and save your own configurations, start with a copy the supplied configuration file and delete the labels you don't need, rather than building a configuration from scratch.

There are some characteristics of the supplied configuration file that you should be aware of:

- The data bus is split between two labels. This is necessary because the logic analyzer allows only 32 bits to be assigned to a label.
- To save a configuration, be sure to save the whole workspace, not just the logic analyzer configuration. This is necessary because the measurement setup spans several parts of the workspace, including several logic analyzer "machines" and the merge tool.

**See Also**

See the online help for general information on modifying, saving, and loading configuration files.

## To load an inverse assembler

Disassembly for the Intel® 423-pin IA-32 processor can be provided through American Arium and connection to the WinDb debugger. See the debugger documentation for more information.

Contact American Arium at:

American Arium
14811 Myford Road
Tustin, CA 92780

877-508-3970
714-731-1661

www.arium.com

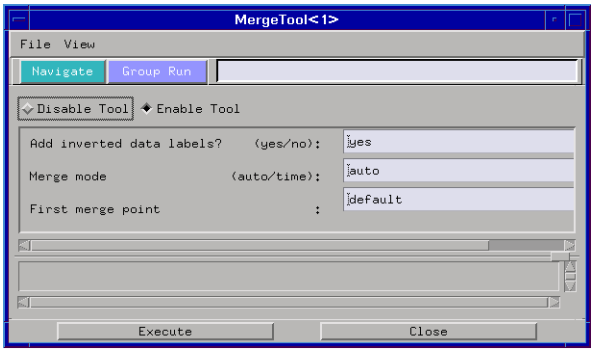
# Setting Merge Tool Preferences

The default settings work well in most situations. If you need to make changes:

1 Make sure the appropriate configuration file has been loaded.

2 Open the Workspace window.

3 Select the Merge tool.




4 Set the preferences as follows:

**Add inverted data labels?** Enter `yes` (the default) if you want the Merge tool to output additional data labels which are inverted as needed to show the actual data values.

Enter `no` if you you do not want the inverted data labels (that is, if you *only* want to see data with the polarity as found on the front side bus).

**Merge mode.** Enter `auto` (the default) if you want the merge tool to automatically switch to merging by state when the traces from both machines end at state 0. Otherwise, the tool will merge by time. See “Capturing Data When the Processor Hangs” on page 72.

Enter `time` if you need to set an "end" trigger which may cause both listings to end with state 0. (This is rarely necessary...even with the trigger set to "end", most traces run a few states past 0.)

**First merge point.** Do not change. Reserved for Agilent use.

# Loading Symbol Information

Symbols are more easily recognized than hexadecimal address values in logic analyzer trace displays, and they are easier to remember when setting up triggers.

Agilent logic analyzers let you assign user-defined symbol names to particular label values.

Also, you can download symbols from certain object file formats into Agilent logic analyzers.

## To view predefined symbols for the IA-32

User-defined symbols are symbols you create in the logic analyzer by assigning symbol names to label values. Typically, you assign symbol names to address label values, but you can define symbols for data, status, or other label values as well.

User-defined symbols are saved with logic analyzer configurations. The supplied logic analyzer configuration files contain predefined symbols for logic analyzer labels.

To display the predefined symbols:

1. Open the logic analyzer's Setup window.
2. Select the Symbols tab.
3. Select the User Defined Symbols tab.
4. Choose a label name from the "Label" list.

   The logic analyzer will display the symbols associated with the label.

## To load object file symbols

The most common way to load program symbols into the logic analyzer is from an object file that is created when the program is compiled. The object file containing symbolic debug information must be in a format the logic analyzer understands.

If your compiler generates object files in a format that the logic analyzer doesn't understand, you can use a General-Purpose ASCII (GPA) symbol file (see "General-Purpose ASCII (GPA) Symbol File Format" on page 115).

To load symbols in the Agilent 16700-series logic analysis system:

1. Open the logic analyzer module's Setup window.
2. Click the Symbol tab.
3. Click the Object File tab.

   Make sure the label is ADDR.

   From this dialog you can select object files and load their symbol information.

   When you load object file symbols into a logic analyzer, a database of symbol/line number to address assignments is generated from the object file.

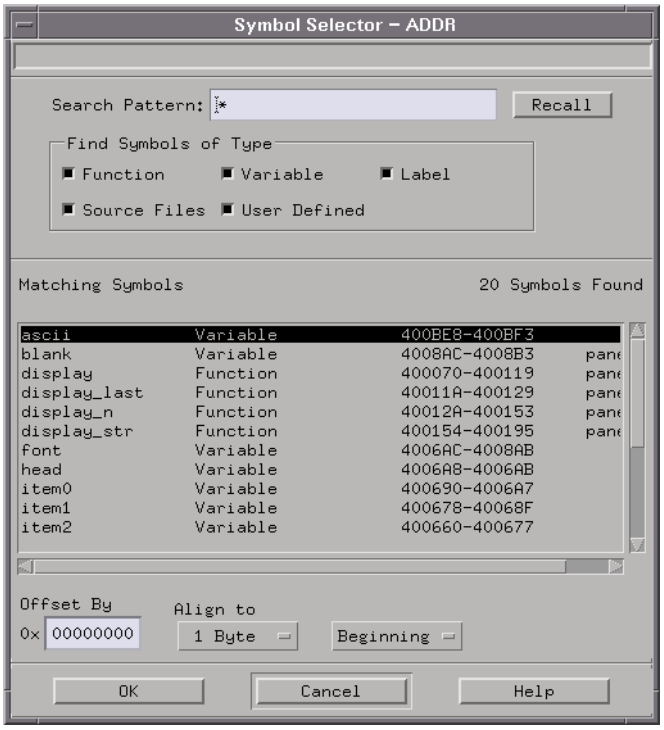
## To access the Symbol Selector dialog:

The Symbol Selector dialog allows you to view the database so you can find a symbol to use in place of a hexadecimal value when defining trigger patterns, trigger ranges, and so on.

The Symbol Selector dialog may be accessed in various ways. One way to access the Symbol Selector dialog is from the Search tab in the Listing display.

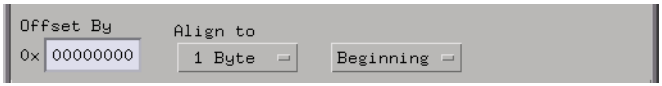
1. Under the Search tab in the Listing display, click Advanced Searching.
2. In the Goto Pattern dialog, click Define.
3. In the Search Pattern dialog, select the Symbols numeric base.
4. Select Pattern, Range, Not Pattern, or Not Range.
5. Click the field to the right of the Pattern/Range selection button.

**6** In the Symbol Selector dialog that appears, select the symbol you want to use.



## To compensate for relocated code

When code segments are relocated, or when memory management units produce fixed code offsets, you can compensate by using the address offset field in the Symbol Selector dialog.




Entering the appropriate address offset will cause the logic analyzer to reference the correct symbol information for the relocatable or offset code.

# Setting Up Labels for Groups of Signals

## Predefined Label Descriptions

The logic analyzer configuration file automatically sets up labels for most microprocessor signals.

Labels which correspond to processor signals are displayed in upper case.

Labels which for signals which are generated by the analysis probe are generally displayed in lower case.

Some of the generated signals include:

### DB_IDLE

Also called databusidle. This signal is used by the Merge tool.

### GC signals

Internal use by the logic analysis software only.

**See Also** For a list of all of the signals, see “Signal-to-connector mapping” on page 98.

## To define additional labels

1. Open the Setup window.
2. Click the Format tab.
3. Click a label and select Insert before... or Insert after....
4. Click the signals under the appropriate pod, then select which bits to include in the label.

# Configuring Signal Thresholds

**Do not change the signal thresholds or set-up and hold times.**

Remember that the logic analyzer is connected to the analysis probe. Changing these parameters will only disrupt the communication between the analysis probe and the logic analyzer—it will not affect how the analysis probe acquires signals from the processor.

6

# Capturing Execution

This chapter shows you how to set up logic analyzer triggers to capture just the data you want.

The normal steps in using the logic analyzer are:

1. Configure the logic analyzer.
2. Format labels for the logic analyzer channels (that is, mapping logic analyzer channels to target system signal names).
3. Load symbols from the program's object file.
4. Set up the trigger, and run the measurement.
5. Display the captured data.

The logic analyzer is configured, and labels are created (formatted) for the logic analysis channels when configuration files are loaded (see "Loading Configuration Files" on page 51).

You can load program object file symbols into the logic analyzer when configuring it (see "Loading Configuration Files" on page 51).

This chapter describes setting up logic analyzer triggers. See Chapter 7, "Displaying Captured States," beginning on page 73 for information on displaying captured data.

**Note: The screens you see may be different from what you see in this manual, depending on the version of your logic analyzer system software.**

# Setting Up Logic Analyzer Triggers

## Triggering on 64-bit data

Triggering on a 64-bit data word is not currently possible. To do this, one would have to set up the trigger to recognize each permutation of inverted and non-inverted data, which would consume all of the analyzer's triggering resources.

## Triggering on 16-bit data

Set up a trigger to recognize both the desired 16-bit value and its inverse.

## Triggering on address or control signals

There are no unusual restrictions for triggering on address values or control signals.

## Triggering on address or control signals and 16-bit data

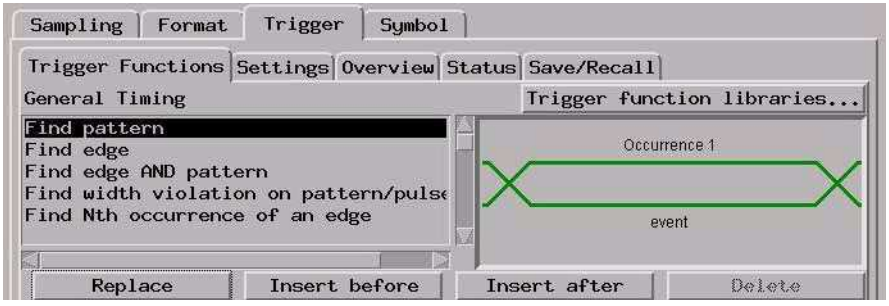
The address and control signals are captured by one machine (the group of cards in the main frame) and the data signals are captured by another machine (the group of cards in the expander frame). Therefore, you must cross-trigger between the two machines. This cross-triggering introduces a delay of approximately 100 ns. For general information on cross-triggering, select the Help button in the main logic analysis system window, then scroll down to "The Intermodule Window."

## To set up logic analyzer triggers

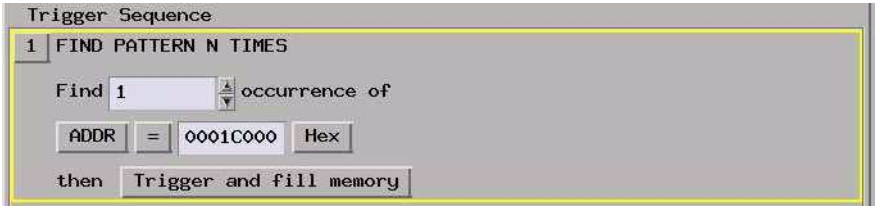
**1** Open the logic analyzer's Setup window.


**2** Select the Trigger tab.


**3** Select the trigger function that will be used in the logic analysis measurement and press the **Replace** button.




**4** Define the patterns, ranges, and other resources that will be used in the logic analysis measurement.



**5** Run the measurement.


**See Also**

The Agilent 16700-series logic analysis system's on-line help for more information on setting up logic analyzer triggers.

# Choosing Which States to Store

You can increase the amount of data captured by the analyzer, and make the listing display easier to read, by using **storage qualification** to store only selected kinds of states. For example, you can configure the analyzer to not store idle states.

Storage qualification can be set up using a combination of:

- the Store Qualifier switch on the front panel of the analysis probe, and
- the default storing configuration in the logic analyzer's Setup window.

## cqual bits

The cqual1# and cqual2# bits are used to qualify BCLK for the address and control machine. (The AND of these bits appears as the Cqual# label.)

When the analysis probe is placed in expanded mode, cqual1# and cqual2# are inactive for idle states, for multiple reset states, and for consecutive snoop states. This results in the elimination of these states from the trace captured by the analyzer.

## To configure storage qualification to store different kinds of states

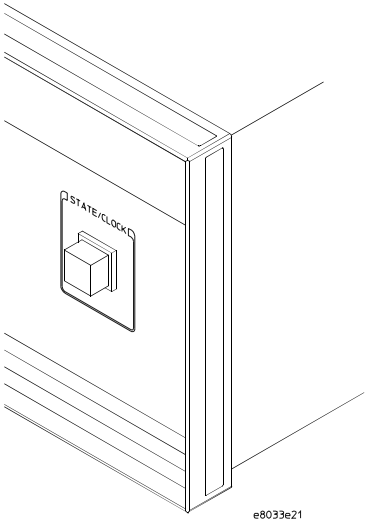
- Set the mode switch and default storing as follows:

| States to be Stored | Store Qualifier Switch | Default Storing |
|---|---|---|
| Store all states | No effect | Disable storage qualification |
| Store all states except:<br>• Idle states | Expanded | Enable storage qualification:<br>store if cqual1# = 0<br>or cqual2# = 0 |
| Store all states except:<br>• Idle states<br>• Consecutive reset states (only the first and last reset states are stored)<br>• Consecutive snoop states (only the last snoop state is stored) | Compacted | Enable storage qualification:<br>store if cqual1# = 0<br>or cqual2# = 0 |

You can turn the clock qualifier off and capture all bus clocks; however, you should not attempt any other storage qualification using the trigger sequence, as that might result in error messages in the listing.

## To set the Store Qualifier switch on the analysis probe

The Store Qualifier mode switch determines when the cqual bits are asserted, as shown in the preceding table.



## To enable storage qualification

The default storing configuration determines whether storage qualification is enabled or disabled.

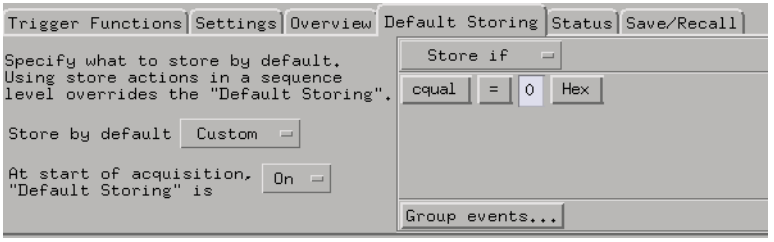
1 Open the Setup window.


2 Select the Trigger tab.

3 Select the Default Storing tab.

4 Set Store by default to Custom.

5 Set the storage qualification to Store if Cqual# = 0.



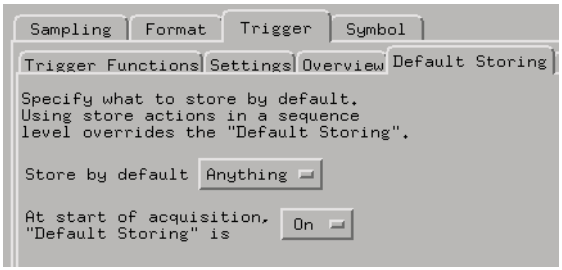

## To disable storage qualification

1 Open the Setup window.


2 Select the Trigger tab.

3 Select the Default Storing tab.

**4** Set Store by default to Anything.



# Triggering on a Transaction Type

## Triggering on address and transaction type

To trigger on a specific address and transaction type, use the A35-32, A31-00, and TranTy labels, together with the TranTy label symbols. The symbols identify each transaction type uniquely, except for Interrupt Acknowledge and Special Transactions, which are combined into one symbol.

## Triggering on data and transaction type

There is no guaranteed method of triggering on a particular transaction type or address ANDed with a particular data value in a target system with overlapping transactions. Alignment in the Listing window is the result of post-processing and cannot be used for triggering. The analysis probe hardware captures this information on different states. A trigger specification could be defined to find a certain transaction type; however, by the time the data pattern is found, it could belong to a different transaction.

# Capturing Data When the Processor Hangs

1 When the processor seems to have hung during a trace measurment, select the Stop Group Run button.

2 The merge tool will switch to merging by state, rather than by time, when it detects that both machines have stopped at state 0.

It is possible to force the merge tool to always merge by time. See page 53.

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# Displaying Captured States

This chapter shows how to display, filter, and interpret data which has been captured by the logic analysis system.

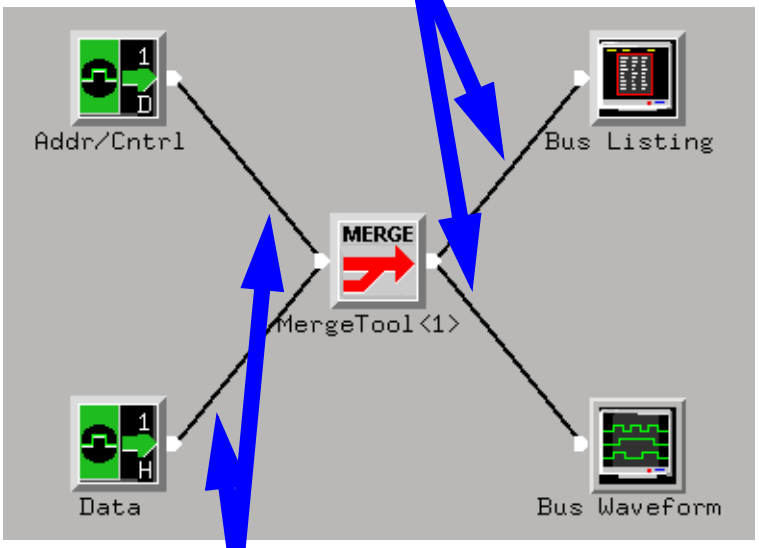
## Understanding the workspace

The Workspace window shows the relationship between the parts of your measurement setup:

The Address/Control machine outputs raw data from the 3 logic analyzer cards in the main frame. A trigger in this machine will trigger the Data machine.

Merged data, so display tools can display both data and address/control signals.

The Listing window shows bus transactions in a readable form.




The Data machine outputs raw data from the 5 logic analyzer cards in the expander frame.

Raw data from analysis probe. Includes "extra" signals generated by the analysis probe for use by the merge tool software. Generally, you should not connect a display tool (Listing or Waveform window) directly to the machines.

The Waveform window shows states as waveforms.

**Do not rename the Addr/Crtrl machine or the Data machine.** Changing the names will break the merge tool. You may rename the display tools (which are outputs of the merge tool).

## Data labels

There are three sets of data labels. Labels are limited to 32 bits, so there are 8 labels in each set: 2 labels to hold the upper and lower 32 bits for each of the 4 phases.

### "P" labels

The Data machine uses labels like D63-32_P1. You will see these labels in the Format window of the Data machine. Normally, you will not use these labels.

### "D" labels

The Merge tool always outputs labels like D63-32_1. These labels show data exactly as it is captured by the logic analyzer on the bus.

### "DI" labels

The Merge tool also outputs inverted labels like DI63-32_1. Chunks of data which were inverted on the bus (as indicated by the DBI bits) are re-inverted so that all of the data appears as it would internally to the processor.

If you do not want to use the "DI" labels at all, you can configure the merge tool not to generate them (page 53).

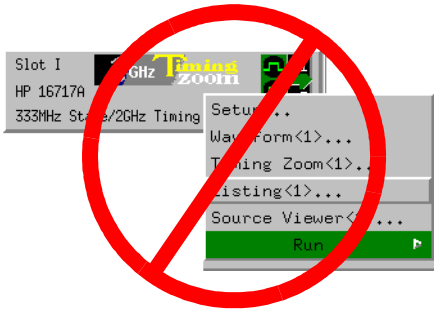
### "DBI" labels

The DBI_4[3:0], DBI_3[3:0], DBI_2[3:0], and DBI_1[3:0] bits indicate whether the a particular 16-bit chunk of data is inverted on the bus. For example, if DBI_3[2] = 1, the data in the lower 16 bits of the D63-32_3 label is inverted on the bus.

## To display the captured data

1 In the Workspace window, connect a Listing display to the output of the Merge tool.

Opening the Listing or Waveform displays from the main window will bypass the Merge tool and directly access the Data or Control/Address machine.

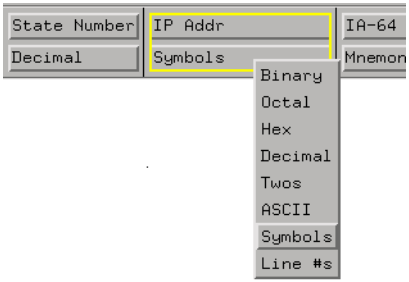



**See Also**

The Agilent 16700-series logic analysis system on-line help for information on using the Listing display.

## To display symbols

- In the Listing window, select the label base and select Symbols.




You can display a label in symbolic form, if you have defined symbols for that label. Any symbols that have been defined will be displayed in place of the captured values.

For example, if your compiler or assembler outputs a symbol file, you can display IP addresses in terms of the modules and functions in your source code.

**See Also**

"Loading Symbol Information" on page 54

"Loading Configuration Files" on page 51.

# Displaying Signals as Waveforms

## To display timing information

The Agilent E8033A does not support asynchronous timing analysis. However, you can use the Waveform window to display the timing relationship of various signals relative to their sampling with BCLK.

To capture these waveforms:

1. Set the operating mode to State-per-clock with Expanded Clock Qualifier
2. Turn off the clock qualifier using the Master Clock field in the Format menu.
3. In the Workspace window, connect a Waveform tool to the output of the Merge tool, as shown on page 74.

> Opening the Listing or Waveform displays from the main window will bypass the Merge tool and directly access the Data or Control/Address machine.

You can also use the Waveform display in the state analysis mode to display state timing diagrams.

## To display a waveform with the correct polarity

There are two sets of data labels. It is important to select the appropriate labels for your needs:

- The "D" labels display each signal with the actual polarity which appears at the pins of the processor.
- The "DI" labels generated by the Merge tool re-invert the data bits as necessary so that they are all shown with the same polarity.

# Filtering Information in the Listing

The filtering options allow you to display or hide certain types of microprocessor bus cycles.

Because the filter options do not affect the data that is stored by the logic analyzer (they only affect whether that data is displayed), they let you display the same data in different ways.

Filtering allows faster analysis in two ways:

- Unneeded information can be taken out of the display.
- Particular operations can be isolated by suppressing all other operations. For example, code reads can be shown, with all other states suppressed, allowing quick analysis of program activity.

You can also use color to distinguish between cycle types (when they are displayed). Color can be used for distinguishing between memory bank accesses or cycle types, but not both at the same time.

# Using Other Tools to Process and Display Your Data

## Useful tools

Some tools in your logic analysis system which are useful for IA-32 analysis include:

**Chart Tool.** For displaying x-y plots of various data values.

**Compare Tool.** For comparing a "golden trace" from a known-good target system to a trace from another target system.

**Distribution Tool.** For displaying an overview of activity in a bar-graph form.

**Pattern Filter.** For excluding selected data from a data stream before you view it or store it.

**System Performance Analyzer.** (Licensed separately.) For displaying the distribution of bus events in time, for visually identifying patterns of activity, and for identifying operations which consume significant system resources.

**Tool Development Kit.** (Licensed separately.) For writing programs to postprocess data in any way you like.

**American Arium WinDb debugger.** For inverse assembly.

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# Troubleshooting the Analysis Probe

This chapter explains how to solve problems you could encounter when you use the analysis probe.

# Troubleshooting the Analysis Probe

If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Agilent Technologies service center.

**CAUTION:** When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

# Logic Analyzer Problems

This section lists general problems that you might encounter while using the logic analyzer.

## Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ❏ Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.
- ❏ Check that the analysis probe cables and logic analyzer cables have not been physically damaged or kinked.
- ❏ Use an oscilloscope to check the signal integrity of the data lines.

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

**See Also**

See *Capacitive Loading* in this chapter for information on other sources of intermittent data errors.

## Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ❏ Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

## No activity on activity indicators

- ❏ Check for loose cables, board connections, and analysis probe connections.
- ❏ Check for bent or damaged pins on the analysis probe.

## No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ❏ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ❏ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

# Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Agilent Technologies Sales Office if you need further assistance.

## Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

❏ Ensure that you are following the correct power-on sequence for the analysis probe and target system.

**1** Power up the analyzer and analysis probe.

**2** Power up the target system.

If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

❏ Verify that the microprocessor and the interposer are securely inserted into their respective sockets.

❏ Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.

❏ Remove any extra sockets (pin protectors) which may have been added.

## Erratic trace measurements

❏ Do a full reset of the target system before beginning the measurement.

Some analysis probe designs require a full reset to ensure correct

configuration.

- ❏ Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.

  See *Capacitive loading* in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ❏ Ensure that you have sufficient cooling for the microprocessor.

  Ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

## Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probe add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ❏ Remove as many pin protectors, extenders, and adapters as possible.

# Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

## An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set an oscilloscope module to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- ❏ Adjust the skew in the Intermodule menu.

  You may be able to specify a skew value that enables the event to be captured.

- ❏ Change the trigger specification for modules upstream of the one with the problem.

  If you are using a logic analyzer to trigger an oscilloscope module, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

# Analysis Probe Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

## "Measurement Initialization Error"

This error occurs when the cables between the logic analyzer cards are installed incorrectly.

Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.

**See Also** The *Agilent Logic Analysis Systems Installation Guide*.

## "No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ❏ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

**See Also** Chapter 5, "Configuring the Logic Analysis System," beginning on page 49, describes how to load configuration files.

## "Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

## "Slow or Missing Clock"

- ❏ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system frame. Ensure that the cards are firmly seated.
- ❏ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ❏ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe.

## "Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- ❏ When analyzing microprocessors that fetch only from word-aligned addresses, ensure that the trigger condition is set to look for an opcode fetch at an address corresponding to a word boundary.

# Part 3

# Reference

9

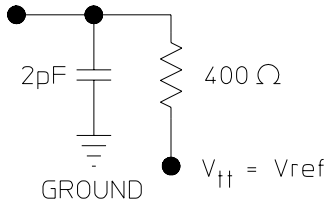
# Hardware Reference

This chapter includes additional reference information including the specifications and characteristics of the analysis probe, as well as signal mapping tables.

# Analysis probe—operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the Agilent E8033A analysis probe.

| Operating Characteristics | |
|---|---|
| **Microprocessor Supported** | Intel® 423-pin IA-32 processor |
| **Clock Frequency** | 100 MHz maximum (BCLK) |
| **Logic Analyzers Supported** | Agilent 16715/16/17/18/19A or 16750/51/52A logic analyzers in an Agilent 16700-series logic analysis system and expander frame. (See page 23 for supported configurations.) |
| **Analysis Probe Modes** | state/clock—expanded mode<br>state/clock—compacted mode |
| **Analysis Probe Cable Length** | Approximately 4 feet |
| **Accessories Required** | |

| Electrical Characteristics | |
|---|---|
| **Power Requirements** | 115/230 Vac, 48-66Hz, 1000W power supply is built into the analysis probe. Line selection is autoranging.<br>CAT II (Line voltage in appliance and to wall outlet)<br>Pollution degree 2 |
| **Signal Line Loading** | GTL+ signals<br>  <br> |

| Environmental Characteristics (Operating) | |
|---|---|
| **Temperature** | 20° to + 30° C (+68° to +86° F) |
| **Altitude** | 4,600 m (15,000 ft) |
| **Humidity** | Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.<br>For indoor use only. |

# Signal-to-connector mapping

The following table defines the logic analyzer bit assignments.

### Key:

**Signal:** Name of the signal coming from the analysis probe into the logic analysis system.

**Phase:** Due to the source synchrounous nature of the bus, data captured by the logic analyzer in four chunks of 64-bit data. In a four-chunk data transfer, the analysis probe maps each of the 4 phases to a separate set of logic analyzer pins.

| Phase | Strobe | Edge |
|---|---|---|
| 1 | P[3:0] | 1st falling edge |
| 2 | N[3:0] | 1st falling edge |
| 3 | P[3:0] | 2nd falling edge |
| 4 | N[3:0] | 2nd falling edge |

For address signals, each of the 2 phases is mapped to a separate logic analyzer pin:.

| Phase | Address strobe |
|---|---|
| 1 | falling edge |
| 2 | rising edge |

**Pod-Bit:** The logic analyzer pod containing the signal and the bit number of the particular pin on the pod.

**Label (Format):** Name of the signal coming from the analysis probe into the logic analysis system, as displayed in the Format window or in a Listing window which is connected directly to the 3-card or 5-card machine. Upper-case signal names generally correspond to signals from the processor. Lower-case signal names are generally signals generated by the analysis probe to allow the inverse assembler to properly decode bus activity.

**Label (after merge):** Name of the signal as displayed in the Listing window after the trace has been processed by the merge tool.

**Inverted:** Indicates whether a signal on the logic analyzer is inverted with respect to the front side bus signal.

# Data signals

Do not change the setup/hold configuration. For all data signals, setup time is configured as -2.000 ns and hold time as 4.500 ns.

Signals D[63:0]# and DBI[3:0]# are captured by the 5 card Logic Analyzer Machine.

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI0# | 1 | J1-16 | DBI_P1 (Label Bit 0) | Yes | DBI_1 (Label Bit 0) | Clock J of LA card J |
| D15# | 1 | J1-15 | D31-00_P1 | Yes | D31-00_1 | |
| D14# | 1 | J1-14 | D31-00_P1 | Yes | D31-00_1 | |
| D13# | 1 | J1-13 | D31-00_P1 | Yes | D31-00_1 | |
| D12# | 1 | J1-12 | D31-00_P1 | Yes | D31-00_1 | |
| D11# | 1 | J1-11 | D31-00_P1 | Yes | D31-00_1 | |
| D10# | 1 | J1-10 | D31-00_P1 | Yes | D31-00_1 | |
| D9# | 1 | J1-9 | D31-00_P1 | Yes | D31-00_1 | |
| D8# | 1 | J1-8 | D31-00_P1 | Yes | D31-00_1 | |
| D7# | 1 | J1-7 | D31-00_P1 | Yes | D31-00_1 | |
| D6# | 1 | J1-6 | D31-00_P1 | Yes | D31-00_1 | |
| D5# | 1 | J1-5 | D31-00_P1 | Yes | D31-00_1 | |
| D4# | 1 | J1-4 | D31-00_P1 | Yes | D31-00_1 | |
| D3# | 1 | J1-3 | D31-00_P1 | Yes | D31-00_1 | |
| D2# | 1 | J1-2 | D31-00_P1 | Yes | D31-00_1 | |
| D1# | 1 | J1-1 | D31-00_P1 | Yes | D31-00_1 | |
| D0# | 1 | J1-0 | D31-00_P1 | Yes | D31-00_1 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI0# | 2 | J2-16 | DBI_P2 (Label Bit 0) | Yes | DBI_2 (Label Bit 0) | Clock K of LA card J |
| D15# | 2 | J2-15 | D31-00_P2 | Yes | D31-00_2 | |
| D14# | 2 | J2-14 | D31-00_P2 | Yes | D31-00_2 | |
| D13# | 2 | J2-13 | D31-00_P2 | Yes | D31-00_2 | |
| D12# | 2 | J2-12 | D31-00_P2 | Yes | D31-00_2 | |
| D11# | 2 | J2-11 | D31-00_P2 | Yes | D31-00_2 | |
| D10# | 2 | J2-10 | D31-00_P2 | Yes | D31-00_2 | |
| D9# | 2 | J2-9 | D31-00_P2 | Yes | D31-00_2 | |
| D8# | 2 | J2-8 | D31-00_P2 | Yes | D31-00_2 | |
| D7# | 2 | J2-7 | D31-00_P2 | Yes | D31-00_2 | |
| D6# | 2 | J2-6 | D31-00_P2 | Yes | D31-00_2 | |
| D5# | 2 | J2-5 | D31-00_P2 | Yes | D31-00_2 | |
| D4# | 2 | J2-4 | D31-00_P2 | Yes | D31-00_2 | |
| D3# | 2 | J2-3 | D31-00_P2 | Yes | D31-00_2 | |
| D2# | 2 | J2-2 | D31-00_P2 | Yes | D31-00_2 | |
| D1# | 2 | J2-1 | D31-00_P2 | Yes | D31-00_2 | |
| D0# | 2 | J2-0 | D31-00_P2 | Yes | D31-00_2 | |
| | | | | | | |
| DBI0# | 3 | J3-16 | DBI_P3 (Label Bit 0) | Yes | DBI_3 (Label Bit 0) | Clock L of LA card J |
| D15# | 3 | J3-15 | D31-00_P3 | Yes | D31-00_3 | |
| D14# | 3 | J3-14 | D31-00_P3 | Yes | D31-00_3 | |
| D13# | 3 | J3-13 | D31-00_P3 | Yes | D31-00_3 | |
| D12# | 3 | J3-12 | D31-00_P3 | Yes | D31-00_3 | |
| D11# | 3 | J3-11 | D31-00_P3 | Yes | D31-00_3 | |
| D10# | 3 | J3-10 | D31-00_P3 | Yes | D31-00_3 | |
| D9# | 3 | J3-9 | D31-00_P3 | Yes | D31-00_3 | |
| D8# | 3 | J3-8 | D31-00_P3 | Yes | D31-00_3 | |
| D7# | 3 | J3-7 | D31-00_P3 | Yes | D31-00_3 | |
| D6# | 3 | J3-6 | D31-00_P3 | Yes | D31-00_3 | |
| D5# | 3 | J3-5 | D31-00_P3 | Yes | D31-00_3 | |
| D4# | 3 | J3-4 | D31-00_P3 | Yes | D31-00_3 | |
| D3# | 3 | J3-3 | D31-00_P3 | Yes | D31-00_3 | |
| D2# | 3 | J3-2 | D31-00_P3 | Yes | D31-00_3 | |
| D1# | 3 | J3-1 | D31-00_P3 | Yes | D31-00_3 | |
| D0# | 3 | J3-0 | D31-00_P3 | Yes | D31-00_3 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI0# | 4 | J4-16 | DBI_P4 (Label Bit 0) | Yes | DBI_4 (Label Bit 0) | Clock M of LA card J |
| D15# | 4 | J4-15 | D31-00_P4 | Yes | D31-00_4 | |
| D14# | 4 | J4-14 | D31-00_P4 | Yes | D31-00_4 | |
| D13# | 4 | J4-13 | D31-00_P4 | Yes | D31-00_4 | |
| D12# | 4 | J4-12 | D31-00_P4 | Yes | D31-00_4 | |
| D11# | 4 | J4-11 | D31-00_P4 | Yes | D31-00_4 | |
| D10# | 4 | J4-10 | D31-00_P4 | Yes | D31-00_4 | |
| D9# | 4 | J4-9 | D31-00_P4 | Yes | D31-00_4 | |
| D8# | 4 | J4-8 | D31-00_P4 | Yes | D31-00_4 | |
| D7# | 4 | J4-7 | D31-00_P4 | Yes | D31-00_4 | |
| D6# | 4 | J4-6 | D31-00_P4 | Yes | D31-00_4 | |
| D5# | 4 | J4-5 | D31-00_P4 | Yes | D31-00_4 | |
| D4# | 4 | J4-4 | D31-00_P4 | Yes | D31-00_4 | |
| D3# | 4 | J4-3 | D31-00_P4 | Yes | D31-00_4 | |
| D2# | 4 | J4-2 | D31-00_P4 | Yes | D31-00_4 | |
| D1# | 4 | J4-1 | D31-00_P4 | Yes | D31-00_4 | |
| D0# | 4 | J4-0 | D31-00_P4 | Yes | D31-00_4 | |
| | | | | | | |
| DBI1# | 1 | I1-16 | DBI_P1 (Label Bit 1) | Yes | DBI_1 (label Bit 1) | Clock J of LA card I |
| D31# | 1 | I1-15 | D31-00_P1 | Yes | D31-00_1 | |
| D30# | 1 | I1-14 | D31-00_P1 | Yes | D31-00_1 | |
| D29# | 1 | I1-13 | D31-00_P1 | Yes | D31-00_1 | |
| D28# | 1 | I1-12 | D31-00_P1 | Yes | D31-00_1 | |
| D27# | 1 | I1-11 | D31-00_P1 | Yes | D31-00_1 | |
| D26# | 1 | I1-10 | D31-00_P1 | Yes | D31-00_1 | |
| D25# | 1 | I1-9 | D31-00_P1 | Yes | D31-00_1 | |
| D24# | 1 | I1-8 | D31-00_P1 | Yes | D31-00_1 | |
| D23# | 1 | I1-7 | D31-00_P1 | Yes | D31-00_1 | |
| D22# | 1 | I1-6 | D31-00_P1 | Yes | D31-00_1 | |
| D21# | 1 | I1-5 | D31-00_P1 | Yes | D31-00_1 | |
| D20# | 1 | I1-4 | D31-00_P1 | Yes | D31-00_1 | |
| D19# | 1 | I1-3 | D31-00_P1 | Yes | D31-00_1 | |
| D18# | 1 | I1-2 | D31-00_P1 | Yes | D31-00_1 | |
| D17# | 1 | I1-1 | D31-00_P1 | Yes | D31-00_1 | |
| D16# | 1 | I1-0 | D31-00_P1 | Yes | D31-00_1 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI1# | 2 | I2-16 | DBI_P2 (Label Bit 1) | Yes | DBI_2 (Label Bit 1) | Clock K of LA card I |
| D31# | 2 | I2-15 | D31-00_P2 | Yes | D31-00_2 | |
| D30# | 2 | I2-14 | D31-00_P2 | Yes | D31-00_2 | |
| D29# | 2 | I2-13 | D31-00_P2 | Yes | D31-00_2 | |
| D28# | 2 | I2-12 | D31-00_P2 | Yes | D31-00_2 | |
| D27# | 2 | I2-11 | D31-00_P2 | Yes | D31-00_2 | |
| D26# | 2 | I2-10 | D31-00_P2 | Yes | D31-00_2 | |
| D25# | 2 | I2-9 | D31-00_P2 | Yes | D31-00_2 | |
| D24# | 2 | I2-8 | D31-00_P2 | Yes | D31-00_2 | |
| D23# | 2 | I2-7 | D31-00_P2 | Yes | D31-00_2 | |
| D22# | 2 | I2-6 | D31-00_P2 | Yes | D31-00_2 | |
| D21# | 2 | I2-5 | D31-00_P2 | Yes | D31-00_2 | |
| D20# | 2 | I2-4 | D31-00_P2 | Yes | D31-00_2 | |
| D19# | 2 | I2-3 | D31-00_P2 | Yes | D31-00_2 | |
| D18# | 2 | I2-2 | D31-00_P2 | Yes | D31-00_2 | |
| D17# | 2 | I2-1 | D31-00_P2 | Yes | D31-00_2 | |
| D16# | 2 | I2-0 | D31-00_P2 | Yes | D31-00_2 | |
| | | | | | | |
| DBI1# | 3 | I3-16 | DBI_P3 (Label Bit 1) | Yes | DBI_3 (Label Bit 1) | Clock L of LA card I |
| D31# | 3 | I3-15 | D31-00_P3 | Yes | D31-00_3 | |
| D30# | 3 | I3-14 | D31-00_P3 | Yes | D31-00_3 | |
| D29# | 3 | I3-13 | D31-00_P3 | Yes | D31-00_3 | |
| D28# | 3 | I3-12 | D31-00_P3 | Yes | D31-00_3 | |
| D27# | 3 | I3-11 | D31-00_P3 | Yes | D31-00_3 | |
| D26# | 3 | I3-10 | D31-00_P3 | Yes | D31-00_3 | |
| D25# | 3 | I3-9 | D31-00_P3 | Yes | D31-00_3 | |
| D24# | 3 | I3-8 | D31-00_P3 | Yes | D31-00_3 | |
| D23# | 3 | I3-7 | D31-00_P3 | Yes | D31-00_3 | |
| D22# | 3 | I3-6 | D31-00_P3 | Yes | D31-00_3 | |
| D21# | 3 | I3-5 | D31-00_P3 | Yes | D31-00_3 | |
| D20# | 3 | I3-4 | D31-00_P3 | Yes | D31-00_3 | |
| D19# | 3 | I3-3 | D31-00_P3 | Yes | D31-00_3 | |
| D18# | 3 | I3-2 | D31-00_P3 | Yes | D31-00_3 | |
| D17# | 3 | I3-1 | D31-00_P3 | Yes | D31-00_3 | |
| D16# | 3 | I3-0 | D31-00_P3 | Yes | D31-00_3 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI1# | 4 | I4-16 | DBI_P4 (Label Bit 1) | Yes | DBI_4 (Label Bit 1) | Clock M of LA card I |
| D31# | 4 | I4-15 | D31-00_P4 | Yes | D31-00_4 | |
| D30# | 4 | I4-14 | D31-00_P4 | Yes | D31-00_4 | |
| D29# | 4 | I4-13 | D31-00_P4 | Yes | D31-00_4 | |
| D28# | 4 | I4-12 | D31-00_P4 | Yes | D31-00_4 | |
| D27# | 4 | I4-11 | D31-00_P4 | Yes | D31-00_4 | |
| D26# | 4 | I4-10 | D31-00_P4 | Yes | D31-00_4 | |
| D25# | 4 | I4-9 | D31-00_P4 | Yes | D31-00_4 | |
| D24# | 4 | I4-8 | D31-00_P4 | Yes | D31-00_4 | |
| D23# | 4 | I4-7 | D31-00_P4 | Yes | D31-00_4 | |
| D22# | 4 | I4-6 | D31-00_P4 | Yes | D31-00_4 | |
| D21# | 4 | I4-5 | D31-00_P4 | Yes | D31-00_4 | |
| D20# | 4 | I4-4 | D31-00_P4 | Yes | D31-00_4 | |
| D19# | 4 | I4-3 | D31-00_P4 | Yes | D31-00_4 | |
| D18# | 4 | I4-2 | D31-00_P4 | Yes | D31-00_4 | |
| D17# | 4 | I4-1 | D31-00_P4 | Yes | D31-00_4 | |
| D16# | 4 | I4-0 | D31-00_P4 | Yes | D31-00_4 | |
| | | | | | | |
| DBI2# | 1 | G1-16 | DBI_P1 (Label Bit 2) | Yes | DBI_1 (Label Bit 2) | Clock J of LA card G |
| D47# | 1 | G1-15 | D63-32_P1 | Yes | D63-32_1 | |
| D46# | 1 | G1-14 | D63-32_P1 | Yes | D63-32_1 | |
| D45# | 1 | G1-13 | D63-32_P1 | Yes | D63-32_1 | |
| D44# | 1 | G1-12 | D63-32_P1 | Yes | D63-32_1 | |
| D43# | 1 | G1-11 | D63-32_P1 | Yes | D63-32_1 | |
| D42# | 1 | G1-10 | D63-32_P1 | Yes | D63-32_1 | |
| D41# | 1 | G1-9 | D63-32_P1 | Yes | D63-32_1 | |
| D40# | 1 | G1-8 | D63-32_P1 | Yes | D63-32_1 | |
| D39# | 1 | G1-7 | D63-32_P1 | Yes | D63-32_1 | |
| D38# | 1 | G1-6 | D63-32_P1 | Yes | D63-32_1 | |
| D37# | 1 | G1-5 | D63-32_P1 | Yes | D63-32_1 | |
| D36# | 1 | G1-4 | D63-32_P1 | Yes | D63-32_1 | |
| D35# | 1 | G1-3 | D63-32_P1 | Yes | D63-32_1 | |
| D34# | 1 | G1-2 | D63-32_P1 | Yes | D63-32_1 | |
| D33# | 1 | G1-1 | D63-32_P1 | Yes | D63-32_1 | |
| D32# | 1 | G1-0 | D63-32_P1 | Yes | D63-32_1 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI2# | 2 | G2-16 | DBI_P2 (Label Bit 2) | Yes | DBI_2 (Label Bit 2) | Clock K of LA card G |
| D47# | 2 | G2-15 | D63-32_P2 | Yes | D63-32_2 | |
| D46# | 2 | G2-14 | D63-32_P2 | Yes | D63-32_2 | |
| D45# | 2 | G2-13 | D63-32_P2 | Yes | D63-32_2 | |
| D44# | 2 | G2-12 | D63-32_P2 | Yes | D63-32_2 | |
| D43# | 2 | G2-11 | D63-32_P2 | Yes | D63-32_2 | |
| D42# | 2 | G2-10 | D63-32_P2 | Yes | D63-32_2 | |
| D41# | 2 | G2-9 | D63-32_P2 | Yes | D63-32_2 | |
| D40# | 2 | G2-8 | D63-32_P2 | Yes | D63-32_2 | |
| D39# | 2 | G2-7 | D63-32_P2 | Yes | D63-32_2 | |
| D38# | 2 | G2-6 | D63-32_P2 | Yes | D63-32_2 | |
| D37# | 2 | G2-5 | D63-32_P2 | Yes | D63-32_2 | |
| D36# | 2 | G2-4 | D63-32_P2 | Yes | D63-32_2 | |
| D35# | 2 | G2-3 | D63-32_P2 | Yes | D63-32_2 | |
| D34# | 2 | G2-2 | D63-32_P2 | Yes | D63-32_2 | |
| D33# | 2 | G2-1 | D63-32_P2 | Yes | D63-32_2 | |
| D32# | 2 | G2-0 | D63-32_P2 | Yes | D63-32_2 | |
| | | | | | | |
| DBI2# | 3 | G3-16 | DBI_P3 (Label Bit 2) | Yes | DBI_3 (Label Bit 2) | Clock L of LA card G |
| D47# | 3 | G3-15 | D63-32_P3 | Yes | D63-32_3 | |
| D46# | 3 | G3-14 | D63-32_P3 | Yes | D63-32_3 | |
| D45# | 3 | G3-13 | D63-32_P3 | Yes | D63-32_3 | |
| D44# | 3 | G3-12 | D63-32_P3 | Yes | D63-32_3 | |
| D43# | 3 | G3-11 | D63-32_P3 | Yes | D63-32_3 | |
| D42# | 3 | G3-10 | D63-32_P3 | Yes | D63-32_3 | |
| D41# | 3 | G3-9 | D63-32_P3 | Yes | D63-32_3 | |
| D40# | 3 | G3-8 | D63-32_P3 | Yes | D63-32_3 | |
| D39# | 3 | G3-7 | D63-32_P3 | Yes | D63-32_3 | |
| D38# | 3 | G3-6 | D63-32_P3 | Yes | D63-32_3 | |
| D37# | 3 | G3-5 | D63-32_P3 | Yes | D63-32_3 | |
| D36# | 3 | G3-4 | D63-32_P3 | Yes | D63-32_3 | |
| D35# | 3 | G3-3 | D63-32_P3 | Yes | D63-32_3 | |
| D34# | 3 | G3-2 | D63-32_P3 | Yes | D63-32_3 | |
| D33# | 3 | G3-1 | D63-32_P3 | Yes | D63-32_3 | |
| D32# | 3 | G3-0 | D63-32_P3 | Yes | D63-32_3 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI2# | 4 | G4-16 | DBI_P4 (Label Bit 2) | Yes | DBI_4 (Label Bit 2) | Clock M of LA card G |
| D47# | 4 | G4-15 | D63-32_P4 | Yes | D63-32_4 | |
| D46# | 4 | G4-14 | D63-32_P4 | Yes | D63-32_4 | |
| D45# | 4 | G4-13 | D63-32_P4 | Yes | D63-32_4 | |
| D44# | 4 | G4-12 | D63-32_P4 | Yes | D63-32_4 | |
| D43# | 4 | G4-11 | D63-32_P4 | Yes | D63-32_4 | |
| D42# | 4 | G4-10 | D63-32_P4 | Yes | D63-32_4 | |
| D41# | 4 | G4-9 | D63-32_P4 | Yes | D63-32_4 | |
| D40# | 4 | G4-8 | D63-32_P4 | Yes | D63-32_4 | |
| D39# | 4 | G4-7 | D63-32_P4 | Yes | D63-32_4 | |
| D38# | 4 | G4-6 | D63-32_P4 | Yes | D63-32_4 | |
| D37# | 4 | G4-5 | D63-32_P4 | Yes | D63-32_4 | |
| D36# | 4 | G4-4 | D63-32_P4 | Yes | D63-32_4 | |
| D35# | 4 | G4-3 | D63-32_P4 | Yes | D63-32_4 | |
| D34# | 4 | G4-2 | D63-32_P4 | Yes | D63-32_4 | |
| D33# | 4 | G4-1 | D63-32_P4 | Yes | D63-32_4 | |
| D32# | 4 | G4-0 | D63-32_P4 | Yes | D63-32_4 | |
| | | | | | | |
| DBI3# | 1 | F1-16 | DBI_P1 (Label Bit 3) | Yes | DBI_1 (Label Bit 3) | Clock J of LA card F |
| D63# | 1 | F1-15 | D63-32_P1 | Yes | D63-32_1 | |
| D62# | 1 | F1-14 | D63-32_P1 | Yes | D63-32_1 | |
| D61# | 1 | F1-13 | D63-32_P1 | Yes | D63-32_1 | |
| D60# | 1 | F1-12 | D63-32_P1 | Yes | D63-32_1 | |
| D59# | 1 | F1-11 | D63-32_P1 | Yes | D63-32_1 | |
| D58# | 1 | F1-10 | D63-32_P1 | Yes | D63-32_1 | |
| D57# | 1 | F1-9 | D63-32_P1 | Yes | D63-32_1 | |
| D56# | 1 | F1-8 | D63-32_P1 | Yes | D63-32_1 | |
| D55# | 1 | F1-7 | D63-32_P1 | Yes | D63-32_1 | |
| D54# | 1 | F1-6 | D63-32_P1 | Yes | D63-32_1 | |
| D53# | 1 | F1-5 | D63-32_P1 | Yes | D63-32_1 | |
| D52# | 1 | F1-4 | D63-32_P1 | Yes | D63-32_1 | |
| D51# | 1 | F1-3 | D63-32_P1 | Yes | D63-32_1 | |
| D50# | 1 | F1-2 | D63-32_P1 | Yes | D63-32_1 | |
| D49# | 1 | F1-1 | D63-32_P1 | Yes | D63-32_1 | |
| D48# | 1 | F1-0 | D63-32_P1 | Yes | D63-32_1 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI3# | 2 | F2-16 | DBI_P2 (Label Bit 3) | Yes | DBI_2 (Label Bit 3) | Clock K of LA card F |
| D63# | 2 | F2-15 | D63-32_P2 | Yes | D63-32_2 | |
| D62# | 2 | F2-14 | D63-32_P2 | Yes | D63-32_2 | |
| D61# | 2 | F2-13 | D63-32_P2 | Yes | D63-32_2 | |
| D60# | 2 | F2-12 | D63-32_P2 | Yes | D63-32_2 | |
| D59# | 2 | F2-11 | D63-32_P2 | Yes | D63-32_2 | |
| D58# | 2 | F2-10 | D63-32_P2 | Yes | D63-32_2 | |
| D57# | 2 | F2-9 | D63-32_P2 | Yes | D63-32_2 | |
| D56# | 2 | F2-8 | D63-32_P2 | Yes | D63-32_2 | |
| D55# | 2 | F2-7 | D63-32_P2 | Yes | D63-32_2 | |
| D54# | 2 | F2-6 | D63-32_P2 | Yes | D63-32_2 | |
| D53# | 2 | F2-5 | D63-32_P2 | Yes | D63-32_2 | |
| D52# | 2 | F2-4 | D63-32_P2 | Yes | D63-32_2 | |
| D51# | 2 | F2-3 | D63-32_P2 | Yes | D63-32_2 | |
| D50# | 2 | F2-2 | D63-32_P2 | Yes | D63-32_2 | |
| D49# | 2 | F2-1 | D63-32_P2 | Yes | D63-32_2 | |
| D48# | 2 | F2-0 | D63-32_P2 | Yes | D63-32_2 | |
| | | | | | | |
| DBI3# | 3 | F3-16 | DBI_P3 (Label Bit 3) | Yes | DBI_3 (Label Bit 3) | Clock L of LA card F |
| D63# | 3 | F3-15 | D63-32_P3 | Yes | D63-32_3 | |
| D62# | 3 | F3-14 | D63-32_P3 | Yes | D63-32_3 | |
| D61# | 3 | F3-13 | D63-32_P3 | Yes | D63-32_3 | |
| D60# | 3 | F3-12 | D63-32_P3 | Yes | D63-32_3 | |
| D59# | 3 | F3-11 | D63-32_P3 | Yes | D63-32_3 | |
| D58# | 3 | F3-10 | D63-32_P3 | Yes | D63-32_3 | |
| D57# | 3 | F3-9 | D63-32_P3 | Yes | D63-32_3 | |
| D56# | 3 | F3-8 | D63-32_P3 | Yes | D63-32_3 | |
| D55# | 3 | F3-7 | D63-32_P3 | Yes | D63-32_3 | |
| D54# | 3 | F3-6 | D63-32_P3 | Yes | D63-32_3 | |
| D53# | 3 | F3-5 | D63-32_P3 | Yes | D63-32_3 | |
| D52# | 3 | F3-4 | D63-32_P3 | Yes | D63-32_3 | |
| D51# | 3 | F3-3 | D63-32_P3 | Yes | D63-32_3 | |
| D50# | 3 | F3-2 | D63-32_P3 | Yes | D63-32_3 | |
| D49# | 3 | F3-1 | D63-32_P3 | Yes | D63-32_3 | |
| D48# | 3 | F3-0 | D63-32_P3 | Yes | D63-32_3 | |

| Signal | Phase | Anlayzer Pod-Bit | Label (Format) | Inverted | Label (after merge ) | Description |
|---|---|---|---|---|---|---|
| DBI3# | 4 | F4-16 | DBI_P4 (Label Bit 3) | Yes | DBI_4 (Label Bit 3) | Clock M of LA card F |
| D63# | 4 | F4-15 | D63-32_P4 | Yes | D63-32_4 | |
| D62# | 4 | F4-14 | D63-32_P4 | Yes | D63-32_4 | |
| D61# | 4 | F4-13 | D63-32_P4 | Yes | D63-32_4 | |
| D60# | 4 | F4-12 | D63-32_P4 | Yes | D63-32_4 | |
| D59# | 4 | F4-11 | D63-32_P4 | Yes | D63-32_4 | |
| D58# | 4 | F4-10 | D63-32_P4 | Yes | D63-32_4 | |
| D57# | 4 | F4-9 | D63-32_P4 | Yes | D63-32_4 | |
| D56# | 4 | F4-8 | D63-32_P4 | Yes | D63-32_4 | |
| D55# | 4 | F4-7 | D63-32_P4 | Yes | D63-32_4 | |
| D54# | 4 | F4-6 | D63-32_P4 | Yes | D63-32_4 | |
| D53# | 4 | F4-5 | D63-32_P4 | Yes | D63-32_4 | |
| D52# | 4 | F4-4 | D63-32_P4 | Yes | D63-32_4 | |
| D51# | 4 | F4-3 | D63-32_P4 | Yes | D63-32_4 | |
| D50# | 4 | F4-2 | D63-32_P4 | Yes | D63-32_4 | |
| D49# | 4 | F4-1 | D63-32_P4 | Yes | D63-32_4 | |
| D48# | 4 | F4-0 | D63-32_P4 | Yes | D63-32_4 | |
| | | H1-16 | Commmon Strobe | | | Strobe Clock Generated by Analysis Probe |
| Following signals are generated by analysis probe and are used by the analysis probe software only. | | | | | | |
| GC_DATA | | H2-15 thru H2-1 | | | | |
| Following Signal Labels are defined by in the Format window for use by the analysis probe software only: | | | | | | |
| STAT2 | | | | | | |

## Address Signals

Do not change the setup/hold configuration. For address signals, setup time is configured as -3.500 ns and hold time as -1.000 ns.

Address A[35:3] signals are captured by the 3 card Analyzer Machine:

A2, A1, A0 are set to logic 0 on the analysis probe to aid in triggering on address.

| Signal | Phase | Pod-Bit | Label (Format) | Inverted | Label (after merge) | Description |
|---|---|---|---|---|---|---|
| A35# | 1 | C4-15 | A35-32_1 | Yes | A35-32_1 | |
| A34# | 1 | C4-14 | A35-32_1 | Yes | A35-32_1 | |
| A33# | 1 | C4-13 | A35-32_1 | Yes | A35-32_1 | |
| A32# | 1 | C4-12 | A35-32_1 | Yes | A35-32_1 | |
| A35# | 2 | C4-11 | A35-32_2 | Yes | A35-32_2 | |
| A34# | 2 | C4-10 | A35-32_2 | Yes | A35-32_2 | |
| A33# | 2 | C4-9 | A35-32_2 | Yes | A35-32_2 | |
| A32# | 2 | C4-8 | A35-32_2 | Yes | A35-32_2 | |

| Signal | Phase | Pod-Bit | Label (Format) | Inverted | Label (after merge) | Description |
|---|---|---|---|---|---|---|
| A15# | 1 | E1-16 | A31-00_1 | Yes | A31-00_1 | |
| A14# | 1 | E1-15 | A31-00_1 | Yes | A31-00_1 | |
| A13# | 1 | E1-14 | A31-00_1 | Yes | A31-00_1 | |
| A12# | 1 | E1-13 | A31-00_1 | Yes | A31-00_1 | |
| A11# | 1 | E1-12 | A31-00_1 | Yes | A31-00_1 | |
| A10# | 1 | E1-11 | A31-00_1 | Yes | A31-00_1 | |
| A9# | 1 | E1-10 | A31-00_1 | Yes | A31-00_1 | |
| A8# | 1 | E1-9 | A31-00_1 | Yes | A31-00_1 | |
| A7# | 1 | E1-8 | A31-00_1 | Yes | A31-00_1 | |
| A6# | 1 | E1-7 | A31-00_1 | Yes | A31-00_1 | |
| A5# | 1 | E1-6 | A31-00_1 | Yes | A31-00_1 | |
| A4# | 1 | E1-5 | A31-00_1 | Yes | A31-00_1 | |
| A3# | 1 | E1-4 | A31-00_1 | Yes | A31-00_1 | |
| | 1 | E1-3 | A31-00_1 | Yes | | (A2 SET TO LOGIC 0, GENERATED BY LAI) |
| | 1 | E1-2 | A31-00_1 | Yes | | (A1 SET TO LOGIC 0, GENERATED BY LAI) |
| | 1 | E1-1 | A31-00_1 | Yes | | (A0 SET TO LOGIC 0, GENERATED BY LAI) |
| | | | | | | |
| A31# | 1 | E2-15 | A31-00_1 | Yes | A31-00_1 | |
| A30# | 1 | E2-14 | A31-00_1 | Yes | A31-00_1 | |
| A29# | 1 | E2-13 | A31-00_1 | Yes | A31-00_1 | |
| A28# | 1 | E2-12 | A31-00_1 | Yes | A31-00_1 | |
| A27# | 1 | E2-11 | A31-00_1 | Yes | A31-00_1 | |
| A26# | 1 | E2-10 | A31-00_1 | Yes | A31-00_1 | |
| A25# | 1 | E2-9 | A31-00_1 | Yes | A31-00_1 | |
| A24# | 1 | E2-8 | A31-00_1 | Yes | A31-00_1 | |
| A23# | 1 | E2-7 | A31-00_1 | Yes | A31-00_1 | |
| A22# | 1 | E2-6 | A31-00_1 | Yes | A31-00_1 | |
| A21# | 1 | E2-5 | A31-00_1 | Yes | A31-00_1 | |
| A20# | 1 | E2-4 | A31-00_1 | Yes | A31-00_1 | |
| A19# | 1 | E2-3 | A31-00_1 | Yes | A31-00_1 | |
| A18# | 1 | E2-2 | A31-00_1 | Yes | A31-00_1 | |
| A17# | 1 | E2-1 | A31-00_1 | Yes | A31-00_1 | |
| A16# | 1 | E2-0 | A31-00_1 | Yes | A31-00_1 | |

| Signal | Phase | Pod-Bit | Label (Format) | Inverted | Label (after merge) | Description |
|---|---|---|---|---|---|---|
| A15# | 2 | E3-16 | A31-00_2 | Yes | A31-00_2 | |
| A14# | 2 | E3-15 | A31-00_2 | Yes | A31-00_2 | |
| A13# | 2 | E3-14 | A31-00_2 | Yes | A31-00_2 | |
| A12# | 2 | E3-13 | A31-00_2 | Yes | A31-00_2 | |
| A11# | 2 | E3-12 | A31-00_2 | Yes | A31-00_2 | |
| A10# | 2 | E3-11 | A31-00_2 | Yes | A31-00_2 | |
| A9# | 2 | E3-10 | A31-00_2 | Yes | A31-00_2 | |
| A8# | 2 | E3-9 | A31-00_2 | Yes | A31-00_2 | |
| A7# | 2 | E3-8 | A31-00_2 | Yes | A31-00_2 | |
| A6# | 2 | E3-7 | A31-00_2 | Yes | A31-00_2 | |
| A5# | 2 | E3-6 | A31-00_2 | Yes | A31-00_2 | |
| A4# | 2 | E3-5 | A31-00_2 | Yes | A31-00_2 | |
| A3# | 2 | E3-4 | A31-00_2 | Yes | A31-00_2 | |
| | 2 | E3-3 | A31-00_2 | Yes | | (A2 SET TO LOGIC 0, GENERATED BY LAI) |
| | 2 | E3-2 | A31-00_2 | Yes | | (A1 SET TO LOGIC 0, GENERATED BY LAI) |
| | 2 | E3-1 | A31-00_2 | Yes | | (A0 SET TO LOGIC 0, GENERATED BY LAI) |
| | | | | | | |
| A31# | 2 | E4-16 | A31-00_2 | Yes | A31-00_2 | |
| A30# | 2 | E4-15 | A31-00_2 | Yes | A31-00_2 | |
| A29# | 2 | E4-14 | A31-00_2 | Yes | A31-00_2 | |
| A28# | 2 | E4-13 | A31-00_2 | Yes | A31-00_2 | |
| A27# | 2 | E4-12 | A31-00_2 | Yes | A31-00_2 | |
| A26# | 2 | E4-11 | A31-00_2 | Yes | A31-00_2 | |
| A25# | 2 | E4-10 | A31-00_2 | Yes | A31-00_2 | |
| A24# | 2 | E4-9 | A31-00_2 | Yes | A31-00_2 | |
| A23# | 2 | E4-8 | A31-00_2 | Yes | A31-00_2 | |
| A22# | 2 | E4-7 | A31-00_2 | Yes | A31-00_2 | |
| A21# | 2 | E4-6 | A31-00_2 | Yes | A31-00_2 | |
| A20# | 2 | E4-5 | A31-00_2 | Yes | A31-00_2 | |
| A19# | 2 | E4-4 | A31-00_2 | Yes | A31-00_2 | |
| A18# | 2 | E4-3 | A31-00_2 | Yes | A31-00_2 | |
| A17# | 2 | E4-2 | A31-00_2 | Yes | A31-00_2 | |
| A16# | 2 | E4-1 | A31-00_2 | Yes | A31-00_2 | |

# Control Signals

Do not change the setup/hold configuration. For most control signals, setup time is configured as 3.500 ns and hold time as -1.000 ns. The signals generated by the analysis probe use setup=2.500 ns and hold=0. The GC_ADDR signals use setup=1.000 ns and hold=1.500 ns.

| Signal | Pod-Bit | Label (Format) | Inverted | Label (after merge) | Description |
|---|---|---|---|---|---|
| **The following control signals are captured on the processor front side bus:** | | | | | |
| PROCHOT# | D1-16 | PROCHOT# | No | PROCHOT# | Clock J of LA card D |
| BPRI# | D1-15 | BPRI# | No | BPRI# | |
| BR0# | D1-11 | BR# (Label Bit 0) | No | BR# (Label Bit 0) | |
| BNR# | D1-10 | BNR# | No | BNR# | |
| IGNNE# | D1-9 | IGNNE# | No | IGNNE# | |
| SMI# | D1-8 | SMI# | No | SMI# | |
| INIT# | D1-7 | INIT# | No | INIT# | |
| A20M# | D1-6 | A20M# | No | A20M# | |
| BPM5# | D1-5 | BPM# (Label Bit 5) | No | BPM# (Label Bit 5) | |
| BPM4# | D1-4 | BPM# (Label Bit 4) | No | BPM# (Label Bit 4) | |
| BPM3# | D1-3 | BPM# (Label Bit 3) | No | BPM# (Label Bit 3) | |
| BPM1# | D1-2 | BPM# (Label Bit 1) | No | BPM# (Label Bit 1) | |
| BPM0# | D1-1 | BPM# (Label Bit 0) | No | BPM# (Label Bit 0) | |
| BPM2# | D1-0 | BPM# (Label Bit 2) | No | BPM# (Label Bit 2) | |

| Signal | Pod-Bit | Label (Format) | Inverted | Label (after merge) | Description |
|---|---|---|---|---|---|
| AP1# | D2-15 | AP1# | No | AP1# | |
| AP0# | D2-14 | AP0# | No | AP0# | |
| RESET# | D2-13 | RESET# | No | RESET# | |
| BINIT# | D2-12 | BINIT# | No | BINIT# | |
| RSP# | D2-11 | RSP# | No | RSP# | |
| RS2# | D2-10 | RS2# | No | RS2# | |
| RS1# | D2-9 | RS1# | No | RS1# | |
| RS0# | D2-8 | RS0# | No | RS0# | |
| ADS# | D2-7 | ADS# | No | ADS# | |
| MCERR# | D2-6 | MCERR# | No | MCERR# | |
| TRDY# | D2-5 | TRDY# | No | TRDY# | |
| DRDY# | D2-4 | DRDY# | No | DRDY# | |
| DBSY# | D2-3 | DBSY# | No | DBSY# | |
| DEFER# | D2-2 | DEFER# | No | DEFER# | |
| HIT# | D2-1 | HIT# | No | HIT# | |
| HITM# | D2-0 | HITM# | No | HITM# | |
| | | | | | |
| THRMTRIP# | C3-16 | THRMTRIP# | No | THRMTRIP# | Clock L of LA card C |
| LINT1/NMI | C3-15 | LINT1/NMI | No | LINT1/NMI | |
| LINT0/INTR | C3-14 | LINT0/INTR | No | LINT0/INTR | |
| SLP# | C3-13 | SLP# | No | SLP# | |
| STPCLK# | C3-12 | STPCLK# | No | STPCLK# | |
| LOCK# | C3-11 | LOCK# | No | LOCK# | |
| TDI | C3-10 | TDI | No | TDI | |
| TDO | C3-9 | TDO | No | TDO | |
| TCK | C3-8 | TCK | No | TCK | |
| TMS | C3-7 | TMS | No | TMS | |
| IERR# | C3-6 | IERR# | No | IERR# | |
| FERR# | C3-5 | FERR# | No | FERR# | |
| TRST# | C3-4 | TRST# | No | TRST# | |
| DP3# | C3-3 | DP3# | No | DP3# | |
| DP2# | C3-2 | DP2# | No | DP2# | |
| DP1# | C3-1 | DP1# | No | DP1# | |
| DP0# | C3-0 | DP0# | No | DP0# | |

| Signal | Pod-Bit | Label (Format) | Inverted | Label (after merge) | Description |
|---|---|---|---|---|---|
| **The following signals are generated by the analysis probe for use by the software only:** | | | | | |
| cqual2# | D3-16 | Not defined in Format window | N/A | Not Defined | Clock L of LA card D. (cqual1# AND cqual2#) is displayed as Cqual# label |
| ppmode | D3-15 | ppmode | N/A | ppmode | Tells SW that analysis probe is in compact or expanded mode |
| - | D3-14 | - | N/A | - | |
| DB_IDLE | D3-4 | DB_IDLE | N/A | DB_IDLE | Agilent use only |
| - | D3-3 | - | N/A | - | |
| - | D3-2 | - | N/A | - | |
| | | | | | |
| cqual1# | D4-16 | Not defined in Format window | N/A | Not Defined | Clock M of LA card D |
| GC_ADDR[15] | D4-15 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[14] | D4-14 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[13] | D4-13 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[12] | D4-12 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[11] | D4-11 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[10] | D4-10 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[9] | D4-9 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[8] | D4-8 | GC_ADDR | N/A | GC_ADDR | See page 58 for description |
| GC_ADDR[7] | D4-7 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[6] | D4-6 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[5] | D4-5 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[4] | D4-4 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[3] | D4-3 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[2] | D4-2 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[1] | D4-1 | GC_ADDR | N/A | GC_ADDR | |
| GC_ADDR[0] | D4-0 | GC_ADDR | N/A | GC_ADDR | |

10

# General-Purpose ASCII (GPA) Symbol File Format

This chapter is a guide to the General-purpose ASCII format, which allows you to create symbol files without the help of a compiler or assembler.

# General-Purpose ASCII (GPA) Symbol File Format

General-purpose ASCII (GPA) format files are loaded into a logic analyzer just like other object files, but they are usually created differently.

If your compiler does not include symbol information in the output, or if you want to define a symbol not in the object file, you can create an ASCII format symbol file.

Typically, ASCII format symbol files are created using text processing tools to convert compiler or linker map file output that has symbolic information into the proper format.

You can typically get symbol table information from a linker map file to create a General-Purpose ASCII (GPA) symbol file.

Various kinds of symbols are defined in different records in the GPA file. Record headers are enclosed in square brackets; for example, [VARIABLES]. For a summary of GPA file records and associated symbol definition syntax, refer to the “GPA Record Format Summary” that follows.

Each entry in the symbol file must consist of a symbol name followed by an address or address range.

While symbol names can be very long, the logic analyzer only uses the first 16 characters.

The address or address range corresponding to a given symbol appears as a hexadecimal number. The address or address range must immediately follow the symbol name, appear on the same line, and be separated from the symbol name by one or more blank spaces or tabs. Ensure that address ranges are in the following format:

```
beginning address..ending address
```

**Example**

```
main    00001000..00001009
test    00001010..0000101F
var1    00001E22              #this is a variable
```

This example defines two symbols that correspond to address ranges and one point symbol that corresponds to a single address.

For more detailed descriptions of GPA file records and associated symbol definition syntax, refer to these topics that follow:

- SECTIONS
- FUNCTIONS
- VARIABLES
- SOURCE LINES
- START ADDRESS
- Comments

## GPA Record Format Summary

```
[SECTIONS]
section_name start..end attribute

[FUNCTIONS]
func_name start..end

[VARIABLES]
var_name start [size]
var_name start..end

[SOURCE LINES]
File: file_name
line# address

[START ADDRESS]
address

#Comments
```

If no record header is specified, [VARIABLES] is assumed. Lines without a preceding header are assumed to be symbol definitions in one of the VARIABLES formats.

**Example**

This is an example GPA file that contains several different kinds of records:

```
[SECTIONS]
prog     00001000..0000101F
data     40002000..40009FFF
common   FFFF0000..FFFF1000

[FUNCTIONS]
main     00001000..00001009
test     00001010..0000101F

[VARIABLES]
total    40002000  4
value    40008000  4
```

```
[SOURCE LINES]
File: main.c
10        00001000
11        00001002
14        0000100A
22        0000101E

File: test.c
 5        00001010
 7        00001012
11        0000101A
```

General-Purpose ASCII (GPA) Symbol File Format

## SECTIONS

```
[SECTIONS]
section_name  start..end  attribute
```

Use SECTIONS to define symbols for regions of memory, such as sections, segments, or classes.

`section_name` A symbol representing the name of the section.

`start` The first address of the section, in hexadecimal.

`end` The last address of the section, in hexadecimal.

`attribute` This is optional, and may be one of the following:

- NORMAL (default)—The section is a normal, relocatable section, such as code or data.
- NONRELOC—The section contains variables or code that cannot be relocated; this is an absolute segment.

**Define sections first**

To enable section relocation, section definitions must appear before any other definitions in the file.

**Example**

```
[SECTIONS]
prog            00001000..00001FFF
data            00002000..00003FFF
display_io      00008000..0000801F  NONRELOC
```

If you use section definitions in a GPA symbol file, any subsequent function or variable definitions must be within the address ranges of one of the defined sections. Functions and variables that are not within the range are ignored.

# FUNCTIONS

```
[FUNCTIONS]
func_name start..end
```

Use FUNCTIONS to define symbols for program functions, procedures, or subroutines.

`func_name` A symbol representing the function name.

`start` The first address of the function, in hexadecimal.

`end` The last address of the function, in hexadecimal.

**Example**

```
[FUNCTIONS]
main      00001000..00001009
test      00001010..0000101F
```

## VARIABLES

```
[VARIABLES]
var_name   start [size]
var_name   start..end
```

You can specify symbols for variables either by using the address of the variable, the address and the size of the variable, or a range of addresses occupied by the variable. If you specify only the address of a variable, the size is assumed to be one byte.

`var_name` A symbol representing the variable name.

`start` The first address of the variable, in hexadecimal.

`end` The last address of the variable, in hexadecimal.

`size` This is optional, and indicates the size of the variable, in bytes, in decimal.

**Example**

```
[VARIABLES]
subtotal     40002000   4
total        40002004   4
data_array   40003000..4000302F
status_char  40002345
```

## SOURCE LINES

```
[SOURCE LINES]
File: file_name
line#  address
```

Use SOURCE LINES to associate addresses with lines in your source files.

`file_name` The name of a file.

`line#` The number of a line in the file, in decimal.

`address` The address of the source line, in hexadecimal.

**Example**

```
[SOURCE LINES]
File: main.c
10        00001000
11        00001002
14        0000100A
22        0000101E
```

## START ADDRESS

```
[START ADDRESS]
address
```

`address` The address of the program entry point, in hexadecimal.

**Example**

```
[START ADDRESS]
00001000
```

## Comments

```
#comment text
```

Use the # character to include comments in a file. Any text following the # character is ignored. You can put comments on a line alone or on the same line following a symbol entry.

**Example**

```
#This is a comment.
```

# Part 4

# Service Guide

# Replacing the Interposer

## To reconnect the analysis probe to the interposer

This section shows how to reconnect the cables from the analysis probe to the connectors on the interposer. Normally, the interposer should remain connected to the analysis probe. You may need to reconnect the cables, however, if you are replacing a damaged interposer.

**CAUTION:** Do not kink the analysis probe cables. Kinking the analysis probe cables will change the calibration, and the analysis probe will have to be returned for repair and recalibration.

- Use the analysis probe which was shipped with the interposer.

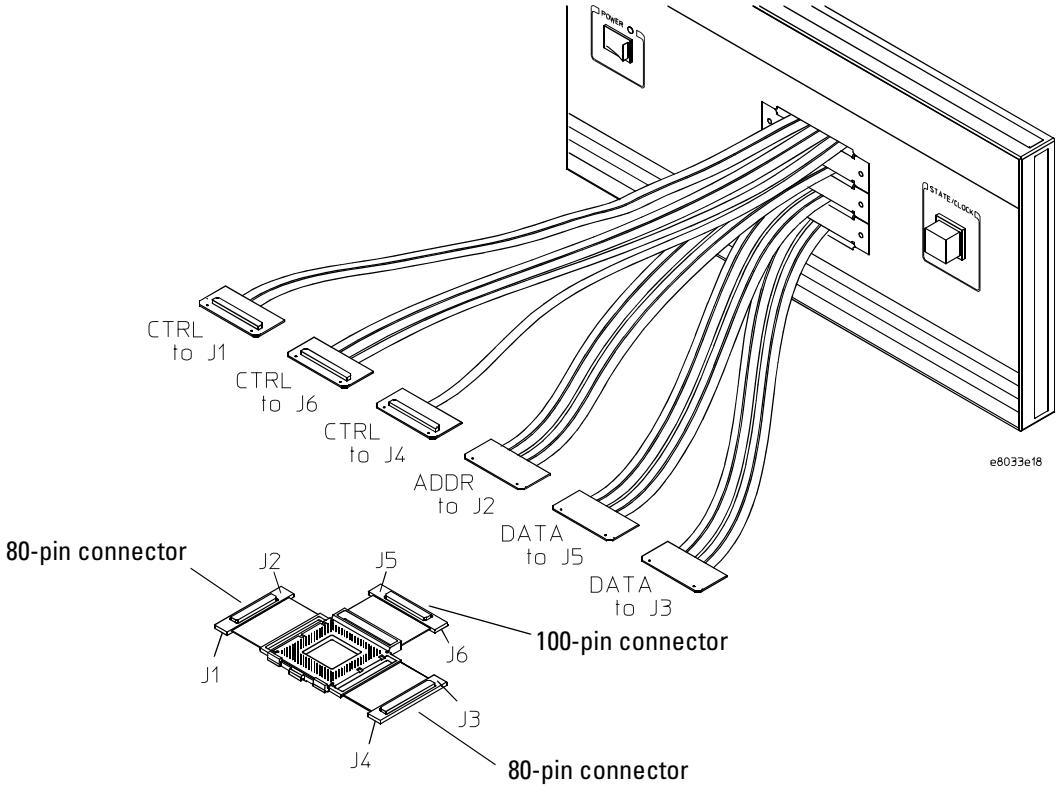
  The analysis probe and interposer are calibrated as a pair.

- Connect the analysis probe cables to the interposer.

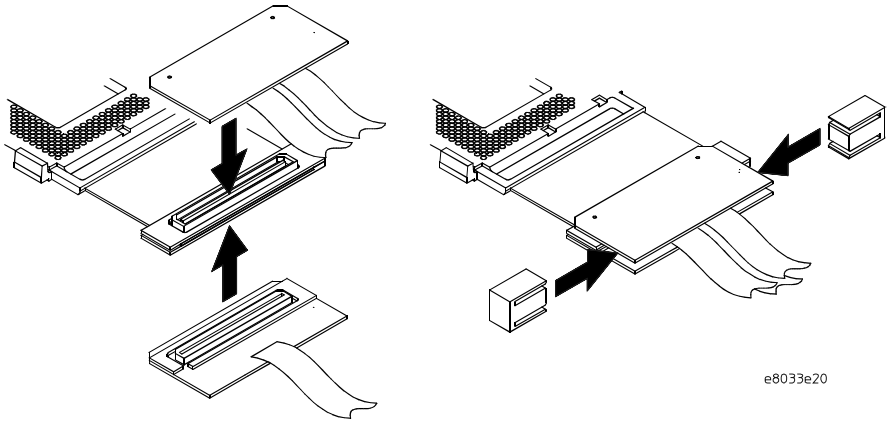
  To make sure you connect the cables in the right place, refer to:

  - the silkscreened labels on the interposer and on the cable paddles (in most situtations, this is the easiest method)
  - the illustration
  - the number of cables going each paddle, as shown in the table

| Signal | Interposer connector | Analysis Probe Cables |
|---|---|---|
| CTRL | J1 | 2 cables |
| CTRL | J6 | 3 cables |
| CTRL | J4 | 1 cable |
| ADDR | J2 | 4 cables |
| DATA | J5 | 4 cables |
| DATA | J3 | 4 cables |


POWER
STATE/CLOCKED
CTRL
to J1
CTRL
to J6
CTRL
to J4
ADDR
to J2
DATA
to J5
DATA
to J3
e8033e18
80-pin connector
J2
J5
J6
J1
J3
J4
100-pin connector
80-pin connector

- The paddles on the end of the analysis probe cables connect to the top and bottom of the interposer wings.
- Install the supplied clips to keep the paddles on the end of the analysis probe cables from pulling apart.



# To return a part to Agilent Technologies for service

1. Follow the procedures in the “Troubleshooting...” chapters to make sure that the problem is caused by a hardware failure, not by configuration or cabling problems.
2. In the U.S., call 1-877-4Agilent (1-877-424-4536). Outside the U.S., call your nearest Agilent sales office. Ask them for the address of the nearest Agilent service center.
3. Package the part and send it to the Agilent service center.

   Keep any parts which you know are working.
4. When the part has been replaced, it will be sent back to you.

   The unit returned to you will have the same serial number as the unit you sent to Agilent.

   The Agilent service center can also troubleshoot the hardware and replace the failed part. To do this, send your entire measurement system to the service center, including the logic analysis system and cables.

   In some parts of the world, on-site repair service is available. Ask an Agilent sales or service representative for details.

# To get replacement parts

The repair strategy for this product is board replacement. However, the following tables list some mechanical parts that may be replaced if they are damaged or lost. Contact your Agilent Technologies Sales Office for further information.

For some parts, exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the “Exchange Assembly” program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

| Agilent Part Number | Description |
|---|---|
| E8033-69001 | Data Interposer |
| E8033-69002 | ITP Interposer |
| E8033-69004 | Analysis Probe Assembly |
| E3435-03801 | Extractor Tool |
| E8033-01101 | Heatsink Spring Clip |
| E8033-24701 | Retention Module Adapter ("Adapter Shim") |
| E8033-24702 | Paddle Board Spacer Clip |
| E8033-60003 | LIF-ZIF Adapter |

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These part numbers are subject to change without notice.

# To clean the instrument

If the instrument requires cleaning:

1. Remove power from the instrument.
2. Clean the instrument with a soft cloth dampened with a mixture of mild detergent and water.
3. Make sure that the instrument is completely dry before reconnecting it to a power source.

**Analysis Probe** A probing solution connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer. Also known as a “preprocessor” or an "LAI."

**Elastomeric Probe Adapter** A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

**Extender** A part whose only function is to provide connections from one location to another. One or more extenders might be stacked to raise a probe above a target microprocessor to avoid mechanical contact with other components installed close to the target microprocessor. Sometimes called a "connector board."

**Flexible Adapter** Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

**General-Purpose Flexible Adapter** A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

**High-Density Adapter Cable** A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

**High-Density Termination Adapter Cable** Same as a High-Density Adapter Cable, except it has a termination in the Mictor connector.

**Inverse Assembler** Software that displays captured bus activity as assembly language mnemonics. In addition, inverse assemblers may show execution history or decode control busses.

**Jumper** Moveable direct electrical connection between two points.

**Label** Labels are used to group and identify logic analyzer channels. A label consists of a name and an associated bit or group of bits.

**LAI** Logic Analyzer Interface, see *Analysis Probe*.

**LIF Socket** Low insertion force socket.

**Mainframe Logic Analyzer** A logic analyzer that resides on one or more board assemblies installed in an Agilent 16500, Agilent 1660-series, or Agilent 16600A/700A-series mainframe.

**Monitor, In** See Background Debug Monitor.

**Preprocessor** See Analysis Probe.

**Probe adapter** See Elastomeric Probe Adapter.

**Setup Assistant** A software program that guides a user through the process of connecting and configuring a logic analyzer to make measurements on a specific microprocessor.

**Shunt Connector.** See Jumper.

**Solution** Agilent's term for a set of tools for debugging a target system.

**Stand-alone Logic Analyzer** A standalone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A standalone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

**Symbol** Symbols represent patterns and ranges of values found on labeled sets of bits. Two kinds of symbols are available:
1) Object file symbols — Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.
2) User-defined symbols — Symbols you create.

**Target Control Port** An 8-bit, TTL port on a logic analysis system that you can use to send signals to your target system. It does not function like a pattern generator or emulation module, but more like a remote control for the target's switches.

**Trigger Specification** A set of conditions that must be true before the instrument triggers. See the printed or online documentation of your logic analyzer for details.

**ZIF Socket** Zero insertion force socket.

**1/4-Flexible Adapter** An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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# Index

# Index

# Agilent Technologies DECLARATION OF CONFORMITY

According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

| | |
|---|---|
| **Manufacturer's Name:** | Agilent Technologies, Inc. |
| **Manufacturer's Address:** | 1900 Garden of the Gods Road<br>Colorado Springs, CO 80907 USA |

**Declares, that the product**

| | |
|---|---|
| **Product Name:** | Analysis Probe / Interposer |
| **Model Number(s):** | E8033A, E8034A, E8040A, E8042A/B (Analysis Probes)<br>E8041A, E8043A/B (Interposers)<br>E8033A/B, E8034A/B, (Base Instrument Model Numbers) |
| **Product Option(s):** | This declaration covers all options of the above product(s). |

**Conforms to the following product standards:**

| | **Standard** | **Limit** |
|---|---|---|
| **EMC:** | IEC 61326-1:1997+A1:1998 / EN61326-1:1997+A1:1998 | |
| | CISPR 11:1990 / EN 55011:1991 | Group 1, Class A[1] |
| | IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995 | 4 kV CD, 8 kV AD |
| | IEC 61000-4-3:1995 / EN 61000-4-3:1995 | 3V/m, 80-1000 MHz |
| | IEC 61000-4-4:1995 / EN 61000-4-4:1995 | 0.5kV signal lines, 1kV power lines |
| | IEC 61000-4-6:1996 / EN 61000-4-6:1996 | 3V, 0.15-80 MHz |
| | Canada: ICES-001:1998 | |
| | Australia/New Zealand: AS/NZS 2064.1 | |
| **Safety:** | IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995<br>Canada: CSA C22.2 No. 1010.1:1992 | |

**Conformity / Supplemental Information:**

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC and carries the CE marking accordingly (European Union).

[1]This product was tested in a typical configuration with Agilent Technologies test systems.

Date: 7/20/2001

Name Ken Wyatt / Product Regulations Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor.

## Product Regulations

| | | |
|---|---|---|
| **EMC** | | Performance Criteria |
| | IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998 | |
| | CISPR 11:1990 / EN 55011:1991 | |
| | IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995 | C (See Note) |
| | IEC 61000-4-3:1995 / EN 61000-4-3:1995 | C |
| | IEC 61000-4-4:1995 / EN 61000-4-4:1995 | C |
| | IEC 61000-4-6:1996 / EN 61000-4-6:1996 | C |
| | Canada: ICES-001:1998 | |
| | Australia/New Zealand: AS/NZS 2064.1 | |
| **Safety** | IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1994+A2:1995 Canada: CSA C22.2 No. 1010.1:1992 | |

### Additional Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC and carries the CE marking accordingly (European Union).

Performance Criteria:
A PASS - Normal operation, no effect.
B PASS - Temporary degradation, self-recoverable.
C PASS - Temporary degradation, operator intervention required.
D FAIL - Not recoverable, component damage.

Note:
The input and output cable assemblies are considered to be ESD sensitive. Use standard ESD preventive practices to avoid component damage.

**Sound Pressure Level** 60 dBA

CE
ISM 1-A

N10149

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**Safety**

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

**Warning**

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock of fire hazard.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

**Safety Symbols**

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

**WARNING**

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

**CAUTION**

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

Agilent Technologies Inc.
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901-2197, U.S.A.

**Product Warranty**

This Agilent Technologies product has a warranty against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Agilent Technologies will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Agilent Technologies.

For products returned to Agilent Technologies for warranty service, the Buyer shall prepay shipping charges to Agilent Technologies and Agilent Technologies shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Agilent Technologies from another country.

Agilent Technologies warrants that its software and firmware designated by Agilent Technologies for use with an instrument will execute its programming instructions when properly installed on that instrument. Agilent Technologies does not warrant that the operation of the instrument software, or firmware will be uninterrupted or error free.

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**Assistance**

Product maintenance agreements and other customer assistance agreements are available for Agilent Technologies products. For any assistance, contact your nearest Agilent Technologies Sales Office.

**Certification**

Agilent Technologies Company certifies that this product met its published specifications at the time of shipment from the factory. Agilent Technologies further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

**About this edition**

This is the *423-Pin IA-32 Processor Analysis Probe User's Guide*.

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Many product updates do not require manual changes, and manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.